Finite-State Predictive Current Control of a Simplified Three-Level Neutral-Point Clamped Inverter

by

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A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Engineering in Electrical and Electronic Engineering

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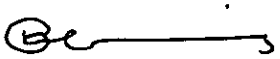
Declaration

This is to certify that the thesis work entitled "*Finite-State Predictive Current Control of a Simplified Three-Level Neutral-Point Clamped Inverter*" has been carried out by *Md. Tariquzzaman* in the Department of *Electrical and Electronic Engineering*, Khulna University of Engineering & Technology, Khulna, Bangladesh. The above thesis work or any part of this work has not been submitted anywhere for the award of any degree or diploma.



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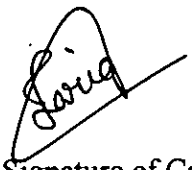

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Abstract

Multilevel inverter is one of the most important parts in renewable energy based power generating section as well as in motor drive applications. The quality of an inverter system depends on current total harmonic distortion (THD), switching loss, fault tolerant ability, dynamic responses, voltage stress, common mode voltage etc. Multilevel inverter yields low current THD, less voltage stress across the semiconductor switches and low switching frequency and thus less switching loss. However, using more number of semiconductor devices and neutral point voltage variation are the common problems for a neutral point clamped inverter. This is why different topologies of multilevel inverter are available in the literature in order to solve the aforementioned problems. The control scheme of a multilevel inverter also plays an important role to guarantee system's performance. Recently, model predictive control (MPC) draws much attention to the researchers for its intuitive features and easy handling of nonlinearities of a system. The controller uses system model to predict the future behavior of the system over a prediction horizon. The control objectives are met by minimizing a predefined cost function that represents the expected behavior of the system. The objective of the proposed research work is to control the output load current of a three level simplified NPC (3L-SNPC) inverter topology using MPC. The simplified NPC inverter is considered, because less number of semiconductor devices used in the topology, even though further investigation is required on different factors such as voltage stress, common mode voltage, losses and switching frequency. MPC is used as controller because it can handle the dc link capacitors voltages balancing problem in a very intuitive way. Moreover, the average switching frequency reduction and over current protection can be easily implemented. Simulation results show that the proposed 3L-SNPC yields similar current THD, transient and steady state responses, voltage stress on the switches at the load side and over current protection capability as the conventional diode clamped based NPC inverter system. The two dc-link capacitor voltages are balanced properly with a neutral point voltage variation of close to zero. However, in comparison with the conventional NPC inverter, the proposed system is 15.25% computationally expensive which yields long execution time and thus less sampling frequency. In this study, two simplified MPC strategies are proposed for the 3L-SNPC inverter system in order to reduce the computational burden: single voltage vector prediction based MPC and selective voltage vector prediction based MPC. Both simplified strategies yield similar performance as the conventional MPC. The required execution times for the simplified MPC strategies are tested on hardware dSPACE 1104 platform. It is found that the single voltage vector prediction based MPC and the selective voltage vector prediction based MPC are computationally efficient by 8.28% and 62.9%, respectively, in comparison with the conventional MPC strategy. However, the average switching frequency and the overall loss in the proposed 3L-SNPC inverter are higher by 83.33% and 46.3%, respectively, than the conventional NPC inverter for a specified load current.

Contents

List of Tables

List of Figures

Nomenclature

$I_L^*(k)$	Reference Load Current at *k*-th Sampling Period
$V_{c1}^*(k)$	Reference Capacitor Voltage at *k*-th Sampling Period
$V_{c1}^*(k)$	Reference Capacitor Voltage at *k*-th Sampling Period
$I_L^p(k+1)$	Predicted Load Current at *k*+1-th Sampling Period
$V_{c1}(k)$	Measured Voltage across Capacitor C_1
$V_{c1}(k)$	Measured Voltage across Capacitor C_2
$I(k)$	Measured Current at *k*-th Sampling Period
$I_a(k)$	'a' Phase Measured Current at *k*-th Sampling Period
$I_b(k)$	'b' Phase Measured Current at *k*-th Sampling Period
V_{DC}	DC link voltage
X	Don't Care Condition
$\boldsymbol{a}$	Unit Vector equals to $e^{j2\pi/3} = -\frac{1}{2} + j\sqrt{3}/2$
N	Neutral Point of Inverter
$V_{aN}, V_{bN}\ and\ V_{cN}$	The Phase-to-Neutral (*N*) Voltages of Inverter
$dv_{c12}^p(k+1)$	Predicted Capacitor Voltage variation at *K*+1-th Sampling Period
T_s	Sampling Time
λ_x	Weighting Factor of '*x*' Constraints
n_{sw}	Number of Switching Transitions
R, L	Per Phase Load Resistance and Inductance
w	Angular Frequency
α	Switching Angle
M	Modulation Index
f_{sw}	Switching Frequency
V_{ce0}	Threshold Voltage of IGBT
T_0	Output Period
$I_x(t)$	IGBT Current in Arm
R_{ce}	IGBT Differential Resistance
$\tau(t)$	Duty Ratio
I_{dc}	DC Link Current

Iccnom, Vccnom	Nominal Current through IGBT and Nominal Voltage Across IGBT during Test
$P_{sw\ instantaneous}$	Instantaneous Switching Loss across IGBT
P_{sw}	Average Switching Loss across IGBT
$Pcon$	Average Conduction Loss
$Pcon_{instantenous}$	Instantaneous Conduction Loss
$P_{harmonic}$	Loss Due to Harmonic
I_{ah}, I_{bh}, I_{ch}	Harmonic Current in a,b,c Phases
I_R, I_Y, I_B	Current of Phase R, Y, B
V_{ab}, V_{bc}, V_{ca}	Line Voltage across the Load
T	Period of a Cycle
I_{THD}	Total harmonic Distortion Current
I_n, V_n	Current and Voltage of n^{th} harmonics

Abbreviations

MLI	Multi-level Inverter
THD	Total Harmonic Distortion
CHB	Cascaded H-bridge
FC	Flying Capacitor
NPC	Neutral Point Clamped
3L-NPC	Three Level Neutral Point Clamped
2L-VSI	Two Level Voltage Source Inverter
MPC	Model Predictive Control
ANPC	Active Neutral Point Clamped
SNPC	Simplified Neutral Point Clamped
3L- SNPC	Three Level Simplified Neutral Point Clamped
PWM	Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
SHE	Selective Harmonic Elimination
PR	Proportional Resonant
FS-MPC	Finite State Model Predictive Control
FCS-MPC	Finite Control State Model Predictive Control
CCS-MPC	Continuous Control State Model Predictive Control
HVDC	High Voltage Direct Current
DVR	Dynamic Voltage Restorers
MMC	Modular Multilevel Converter
KV	Kilo Volt
KVA	Kilo Volt-Ampere
PI	Proportional Integral
SVM	Space Vector Modulation
FOC	Field Oriented Control
VOC	Voltage Oriented Control
DTC	Direct Torque Control
DPC	Direct Power Control
ANN	Artificial Neural Network
FLC	Fuzzy Logic Controller

GPC	Generalized Predictive Control
OSV-MPC	Optimal Switching Vector Model Predictive Control
OSS-MPC	Optimal Switching Sequence Model Predictive Control
MP3C	Model Predictive Pulse Pattern Control
RTI	Real Time Interface
IGBT	Insulated Gate Bipolar Transistor
R-L	Resistive Inductive
FFT	Fast Fourier Transformation

CHAPTER I

Introduction

1.1 Background

Inverters, also known as dc to ac converter, are basically electronic devices which convert dc signals into ac signals. Based on different circuit configurations, inverters can produce square wave, modified square wave, modified sine wave etc. Highly efficient modern power electronics with appropriate control schemes are needed in renewable energy generation systems to enhance system efficiency and to ameliorate output power quality. Multi-level inverters (MLIs) are a lucrative way to meet this growing demand due to their high-quality output current, lower switching losses and less voltage stress on power switches [1]. The quality of output current is improved by increasing the number of output voltage level of inverter and switching frequency. However, higher switching frequency increases switching loss. Hence, a trade off must be made between switching frequency and current total harmonic distortion (THD). A uniform voltage distribution among the switching devices is also desired as it reduces the possibility of insulation breakdown of the switches and, thus enhances their durability.

Recently, multilevel inverters have become a popular choice in comparison with conventional two level inverter for integrating smart grid, ac motor drives applications, reactive power compensation and so on [2]. Multilevel converters possess some attractive features namely less total harmonic distortion in the inverter output current, a suppression in switching stress, a reduction in switching loss, higher voltage operation of the inverter, and required smaller size of interfacing transformers and output filter arrangements [2]-[6].
Different types of multilevel inverter (MLI) topologies are available in literature [7] such as cascaded H-bridge (CHB) inverter, flying capacitor (FC), neutral point clamped (NPC) or diode clamped inverter. Each of the topologies comes with some particular advantages and disadvantages. The three-level neutral-point clamped (3L-NPC) inverter has received increasing interest in medium voltage application after its first introduction in 1981 [8]. Due to its higher efficiency and less harmonic distortion compared to established two-level voltage source inverters (2L-VSIs), the 3L-NPC inverters are also used in low-voltage applications such as high speed and high efficiency electrical drives, and grid connected converters [9], [10]. However, the NPC topology has two main constrains: neutral point voltage balancing and large number of clamping diodes. Moreover, higher switching frequencies are required for balancing capacitor voltages of FC topology which in a sense increase the power loss of the system. CHB topologies require a costly and larger transformer for providing isolated dc sources [3], [4], [6].

To overcome the aforementioned limitations, several modified topologies have been proposed in the literature [11]-[17]. Model predictive control (MPC) based modular multilevel inverter [11], modified version of three level CHB [12], hybrid FC based five level ANPC [13], T-type

NPC [14], [15] have been proposed. A simplified version of NPC has been proposed in [16], [17]. It is shown that simplified NPC has less number of semiconductor switches and diodes in comparison to three level NPC [16].

The control scheme of the MLIs plays an important role to guarantee system stability and enhance efficiency. Different control schemes are available such as pulse width modulation (PWM) [12], space vector pulse width modulation (SVPWM) control [17], selective harmonic elimination PWM (SHE-PWM) [9], model predictive control (MPC) [18], [19] etc.The sinusoidal PWM and SVPWM are the commonly used control strategies, but they suffer from poor THD and poor de-coupled nature. The deadbeat and the sliding mode controls have parameter variation sensitivity, complexity and loading condition problems. However, the controllers yield good dynamic performance in control of the instantaneous inverter output voltage. To suppress the selected harmonics and compensate the reactive power, a hybrid active power filter utilizing proportional-resonant (PR) controller has been developed in [20]. Among the aforementioned control strategies, MPC has drawn significant attention to the power electronic community due to the advancement of microprocessor. The controller uses system model to predict the future behavior of the control parameter. Multiple control parameter can be controlled by solving an optimization problem at each discrete sampling time. The optimization problem means the minimization of a predefined cost function that represents the expected behavior of the system between two successive sampling instants. Predictive control gives the possibility to avoid cascaded structure, which is typically used in the linear control scheme. The other advantages of MPC are fast dynamic response, intuitive handling of multi-variables, nonlinearities and easy inclusion of system constraints [21], [22]. There are two types of MPC in broader sense: finite-state MPC (FS-MPC) and continuous control set MPC (CCS-MPC). In FS- MPC, a finite number of control actions (switching states of inverter) are used, whereas in CCS-MPC, a continuous control signal is computed and a modulator is used to generate the desired output voltage in the power converter. In this research work, the output current of the 3L-SNPC will be controlled using FS-MPC. The MPC controller minimizes the cost function bearing a number of constraints and gives optimum solution at every sample instant. MPC can easily mitigate nonlinearities and restrictions without requiring any linear controllers and modulators [22]-[24]. The details of background studies are covered in chapter II.

The performance parameters for SNPC inverter systems are current THD, neutral point voltage balancing, lower switching frequency, voltage stress and common mode voltage. The permissible amount of harmonics in the output load current of the inverter is presented in Table 1.1 [25].The acceptable limit for range of even harmonics are 25% of those of odd harmonics. It is expected that the proposed system will compel this standard.

Table 1.1: Harmonic distortion limitation set by IEEE 519 [25]

Odd Harmonic Order	Acceptable limit for Odd Harmonic
THD	<5%
3^{rd}-9^{th}	< 4%
11^{th}-15^{th}	< 2%
17^{th}-21^{th}	< 1.5%
23^{rd}-33^{rd}	< 0.6%
> 33^{rd}	< 0.3%

In this research, the output current of a three level SNPC inverter topology is controlled by predicting current tracking error. Similarly, for capacitor voltages balancing, two capacitor voltages are predicted, and the number of switching transitions is predicted for switching frequency reduction. The performance of the proposed simplified topology is compared with the conventional NPC inverter in terms of two important factors: THD and neutral point voltage balancing [21]. As the number of switching devices is reduced in SNPC, it leads to simplify the construction and control scheme of the proposed system.

1.2 Motivation behind this Research Work

The attractive features of the NPC inverter have encouraged the researchers to apply multilevel converter concepts in different power electronics applications. However, the NPC has some inherent limitations which encourage researchers to find out modified version. Among them, SNPC is one of the variants which requires less number of components as well as provides multilevel facilities namely good output load current THD, better balancing ability of capacitor voltages, and enhances reliability. However, very few researches have conducted their research in this context. Therefore, the features of SNPC encourage me to analyze and compare its performance with its ancestor for checking its feasibility.

The control scheme selection is one of the vital factors for smooth operation of power converters. With the rapid advancement of microprocessor, MPC scheme is best suited for this research work as the number of control objectives and constraints that have been dealt with in this research are large. Moreover, FCS-MPC is very intuitive in nature and easily understandable as well as it does not require any modulation block. For this reason, FCS-MPC based SNPC inverter is designed and analyzed. Moreover, improvement in execution time of MPC is performed in this study as it plays an important role for hardware implementation.

1.3 Objectives of this Research

The main objectives of the proposed research work are given below.

i) To implement model predictive control (MPC) based load current control of a three level simplified NPC (3L-SNPC) inverter.

ii) To overcome neutral-point voltage variation problem of a three-level inverter by only considering two measured dc-link voltages.

iii) To improve current ripple by introducing delay compensation method.

iv) To analyze the output current THD, switching loss, transient response, common mode voltage, and voltage stress for MPC based SNPC as well as for MPC based conventional NPC inverter.

v) To reduce the computational burden of the proposed MPC algorithm for the simplified NPC using voltage vector prediction based MPC and selective voltage vector based MPC.

1.4 Dissertation organization

The research work presented in this thesis is organized into five chapters. The work that is carried out in each chapter is summarized below.

Chapter I presents the background study of performing the research work and its importance for the future power electronics applications. The research objectives and dissertation organization are also presented in this chapter.

Chapter II presents the background study of the research work which includes the characteristics, classification and comparative studies of the power inverter, existing control strategies for the converter, suitability of the proposed controller, and its basic operating strategy along with pros and cons. This chapter also presents a key statistics of existing research works to show why the research work is chosen and the importance of it in the field of power and energy technology.

Chapter III presents the methodology of the research work and the system modeling part. In this chapter, the SNPC and NPC inverter modeling, the proposed MPC controller modeling with delay compensation are presented in detail. The mathematical expressions of power loss analysis for the proposed controller are presented. Two simplified techniques of the proposed controller are also discussed in the end of this chapter.

Chapter IV provides the simulation results for the model presenting in Chapter III, which includes the performance analysis of the proposed SNPC inverter system, comprehensive comparison of it with the conventional NPC, power loss analysis, and simplified versions of the proposed MPC algorithm.

Chapter V presents the conclusions of the work along with the future prospects followed by the references.

CHAPTER II

Literature Review

2.1 Introduction

The goal of the research work is to investigate the performance of a simplified 3L-NPC inverter controlled by model predictive control (MPC). The application of power electronic converter and proper selection of its control strategy is an important factor. Therefore, the characteristics, classification and challenging issues of the power converter, overview of the existing control strategies, and the operation of MPC are discussed in this chapter. Comparative analysis among different inverter topologies are also represented here in order to verify the feasibility of the proposed inverter topology. A comparison with the existing controllers is also done in order to discuss the pros and cons of the MPC. It is expected that MPC would fulfill the modern industrial demand. Different research papers and articles have been studied to understand the current scenario of the controllers and find the research gap and scope of the research work. In short, the purpose of this chapter is to provide a clear picture for the readers who are interested on the recently developed MPC for power converter.

2.2 Power Inverter

Inverter plays an important role in power industry. It has numerous applications such as renewable energy application [26], ac motor drives application [27], [28], multi-phase motor drives [29], induction heating power supply [30], High-voltage direct current (HVDC) [31]-[33], Dynamic voltage restorers (DVR) [34]-[36] etc. Since the medium and high power applications are increased day to day, the importance of multi-level inverter topologies is increased. The overall classification of power inverters are shown in Fig. 2.1.The advantages of multi-level inverter over two level voltage source inverter (VSI) or current source inverter are given below.

i) Easy to handle high power.
ii) Better harmonic performance.
iii) Reduction of voltage stress ($\frac{dv}{dt}$).
iv) Reduction of electromagnetic interference.
v) Have Fault tolerant ability with redundant switching states.

The aforementioned features make it attractive in different applications.

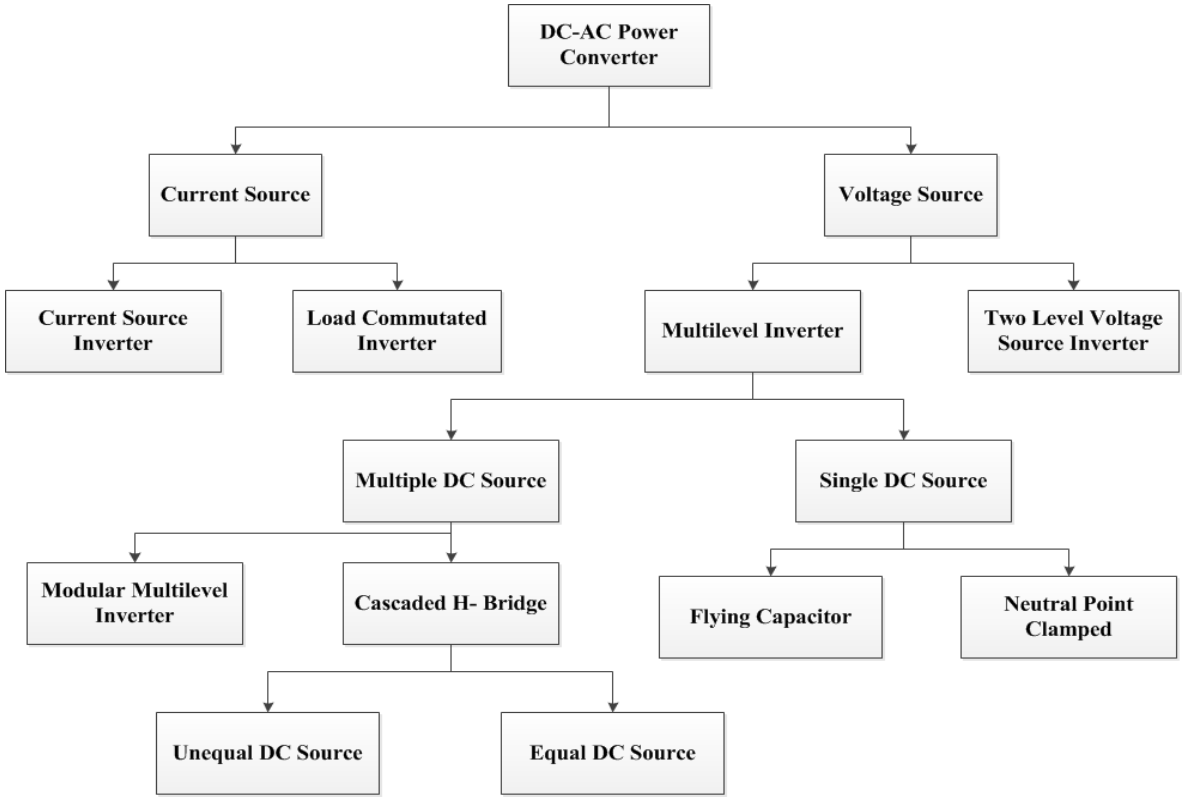


Figure 2.1: Classification of power inverter.

From Fig. 2.1, it is evident that there are mainly four types of multi-level inverter topology. These are the cascaded H-bridge inverter (CHB), modular multilevel converter (MMC), flying capacitor (FC) and neutral point clamped (NPC) inverter. The pros and cons of the four inverters have already been done in literature [37]-[39]. In Table 2.1, the advantages and drawbacks of different multilevel inverter topologies are presented.

Table 2.1: Advantages and drawbacks of different multilevel inverter topologies.

Inverter Topology	Pros	Cons
CHB [40]-[42]	• Appropriate for fault tolerant application. • Asymmetric source configuration can be employed. • Can be designed for high power rating using modular configuration. • Only unidirectional switch is required. • More Reliable and simpler structure.	• More number of gate driver is required. • Large number of separate dc sources are required for increasing the output voltage. • Loss of modularity due to asymmetric configuration. • High implement cost. • Unequal voltage rated semiconductor switches are required.
NPC [8],[43]- [45]	• Better for industrial application. • Reduces the number of DC sources. • Appropriate for fault tolerant application.	• Complex in nature of voltage balancing circuit.

	• Simple design. • Better harmonic spectrum and better dynamic response. • Voltage balancing and the unequal share of losses between switching devices in NPC converters can be solved by neutral clamping switches.	• Unequal share of voltage stress or losses between inner and outer switches. • Require more components to implement.
FC [46]-[48]	• Appropriate for fault tolerant application. • Reduces the number of DC sources. • Require smaller output filter. • Smaller stress on switches.	• Requires large number of electrolytic capacitor. • Poor switching efficiency. • High installation cost
MMC [49],[50]	• Perfect modularity. • Low output harmonic and suitable for all voltage rating. • No need of transformer. • Number of power switching is not increased with the increase of voltage levels.	• Require large number of isolated DC voltage sources. • Voltage imbalance among different phase of inverter. • High voltage ripple through capacitor. • High conduction and thermal loss.

Table 2.1 shows the comparative studies among four different multilevel inverter topologies. Every topology has some pros and cons. Depending on their features and drawbacks, the deployment of the inverter topology is also differed. Normally for high power application, CHB or MMC is mostly used. On the other hand, NPC is adopted for medium power application. It is because the performance of this topology decays when the output voltage rating is more than 4KV [50]. Moreover, NPC is most popular inverter topology for industrial applications.

Though NPC is one of the most popular topologies in industrial application, it suffers to balance the neutral point of the two dc link capacitors. Moreover, it requires large number of diodes, semiconductor devices for implementation, the loss distribution across semiconductor switches are unequal. To overcome the drawbacks, different types of NPC have been studied in literature. Proper selection of control strategy also plays an important role to mitigate the aforementioned problems. Active neutral point clamped [43], T-type neutral point clamped [51] and simplified neutral point clamped [16], [52] are the derived version of the conventional NPC topology. The schematic diagram of each of the modified variant of NPC is shown in Figs. 2.2, 2.3 and 2.4. From Fig. 2.2, the variation of this active neutral point clamped (ANPC) with the NPC with respect to structure is that the clamping diode is replaced by semiconductor switches with anti-parallel diode. This configuration requires higher number of semiconductor switches but it mitigates the unequal loss distribution problem among the switches [43].

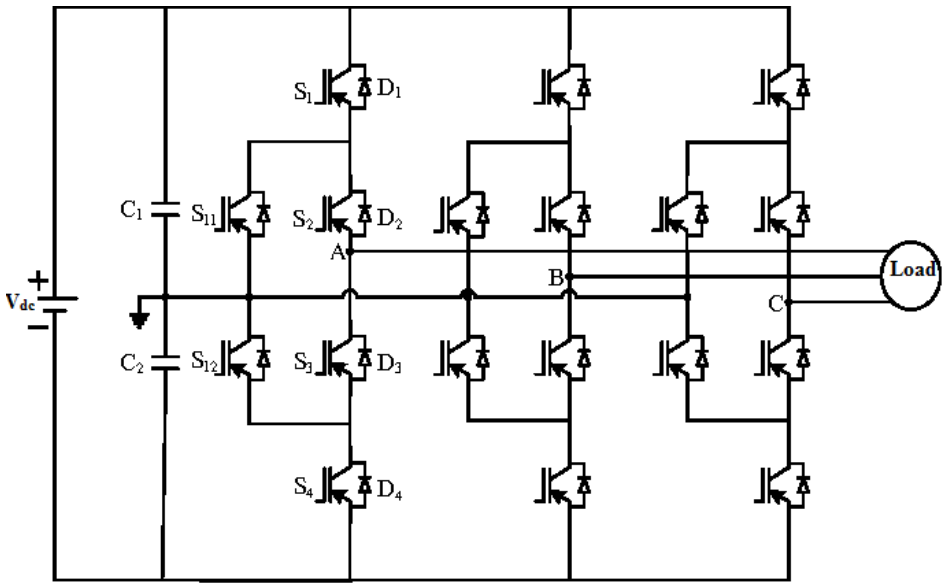


Figure 2.2: Schematic diagram of 3L active NPC inverter [43].

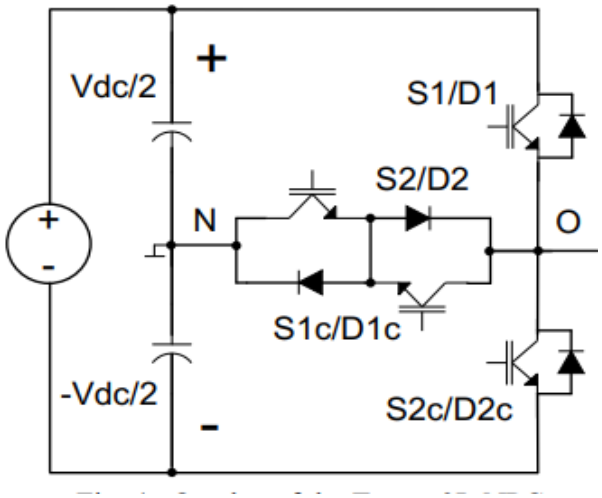


Figure 2.3: Schematic diagram of a single leg of the T-type NPC inverter [51].

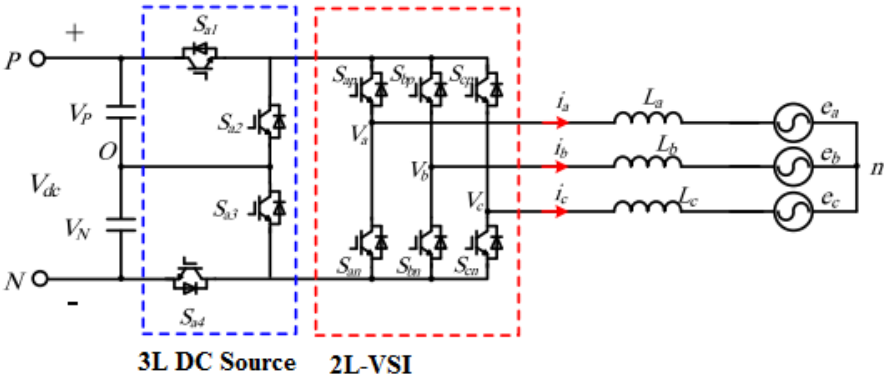


Figure 2.4: Schematic diagram of 3L-simplified NPC inverter [52].

Fig. 2.3 shows the schematic diagram of a single leg T-type NPC variant. It requires less number of diodes as well as reduces conduction loss [51]. Fig. 2.4 illustrates the simplified

version of NPC which requires less number of switches and diodes. This may increase the system reliability from the view point of less number of switches in the topology and ease balancing of capacitor voltages. Of course, some other factors, such as voltage stress, different types of loss, common mode voltage, should also be considered. Hence, further research should be carried out on this topology with one of the modern control strategies. In this research work, simplified NPC (SNPC) inverter is studied, analyzed and compared with the conventional NPC in order to check the feasibility of this variant. It is be expected that the proposed system will perform well enough to use in industrial application. However, for better performance, proper selection of control scheme is crucial, which is discussed in the next section.

2.3 Types of control strategies

Efficiency of a power converter is largely dependent on the used control strategy used for it. Hence, extensive research works have been going on the efficient control strategy for the power converters and new strategies are developed in every year. Some of these control strategies are described below.

2.3.1 Linear Control

The linear controllers of the power converter always consist of a modulating stage. By producing the control signals for the control switches, this modulating device actually linearizes the nonlinear converter control strategy. Proportional-integral (PI) controller is the most widely recognized linear controller. In this method, a reference sinusoidal signal is compared with a triangular carrier signal to produce a PWM signal for the switching device. For instance, when the prompt value of the carrier is not as much as that of the reference signals, the switch state is changed with the goal that the output signal increments, and vice-versa [4]. Apart from this modulation method, some other techniques are available in the literature such as space vector modulation (SVM) and selective harmonic elimination (SHE) [53]. Using the SVM/PWM, a linear controller has been presented in Fig. 2.5, for the current control of the system, where the reference load currents are compared with the measured one and the error found between them is processed by the traditional PI modulators.

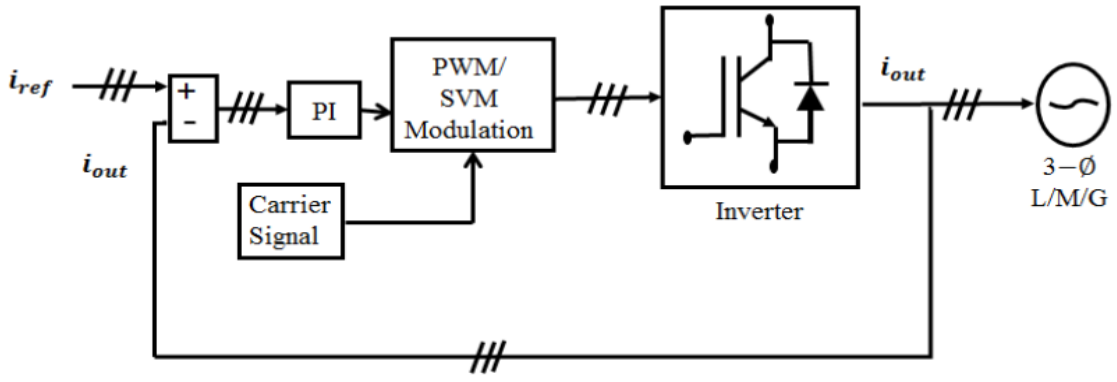


Figure 2.5: PI controller based linear current controller using PWM/SVM for a three-phase load [54].

The SVM is perceived as an effective strategy as it offers lower total harmonic distortion (THD) and improved dc-link voltage usage in contrast with the PWM [54]. With the SVM, the nearest vectors to the reference voltage vector are chosen dependent on dwell time figuring and switching structure [55]. On the other hand, the SVM includes several steps of designing the

model and the model is a little bit complex, which prompts a higher computational burden in contrast with the PWM. The SHE is mostly dependent on the calculation of switching angles to such an extent that particular lower order harmonics can be eliminated [56] and reduce the drawbacks of the previous SVM controller [57]. The switching frequency of the linear controllers utilizing these PWM/SHE/SVM modulating techniques is fixed and the value of error is minimal if the Park's transformation or dq co-ordinate system is utilized in contrast to the αβ transformations co-ordinates. The PI parameters are intended for one working condition, and if the converter works at different working conditions, the performance of the control crumbles and the stability of the system is being questioned [58]. Since this linear controller is applied to the power converter which is nonlinear in nature, the execution acquired is unsymmetrical and it fluctuates by the working condition. The presumption of the linear model gives good execution just if a high bandwidth modulation is utilized. This situation prompts a high switching frequency operation which subsequently causes higher switching losses.

In the area of industrial drive and energy producing system, the linear controllers are extensively utilized. For controlling the flux and torque of the widely used induction motor in a decoupled manner, field oriented control (FOC) is utilized [59]. This control methodology consists of transforming the reference frame, utilization of PI controllers, filtering of output variable and the modulation stage. Similar to this, for controlling the on-grid inverter, voltage oriented control (VOC) is utilized in [59]. This control strategy provides the decoupled feature of grid reactive power and dc-bus voltage.

2.3.2 Hysteresis Control

In hysteresis control, a hysteresis error limit is utilized for determining the switching states by comparing the measured variable to the reference [60] as shown in Fig. 2.6. The switching state is changed when the controlled current achieves the limit.

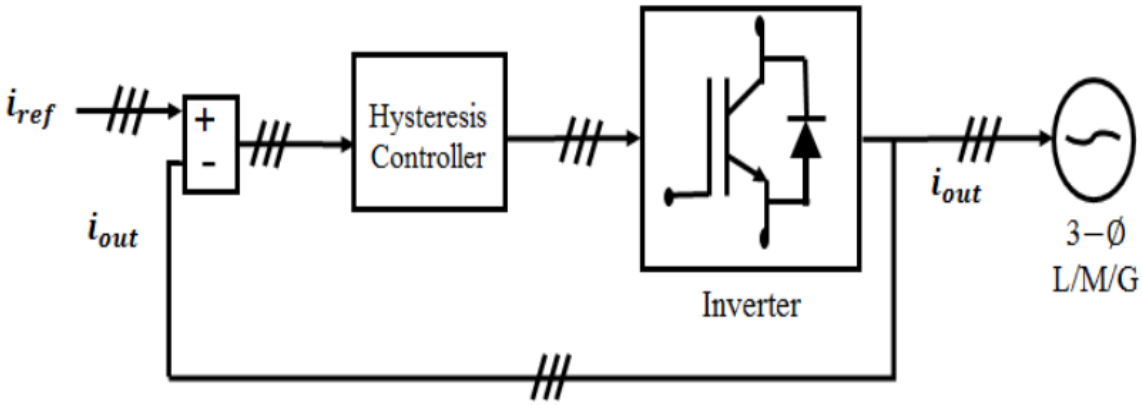


Figure 2.6: Block diagram of three-phase hysteresis current controller for a three-phase load [60].

The application of the strategy is as simple as the current control. However, it can likewise be connected to higher multifaceted nature applications such as direct torque control (DTC) [61] and direct power control (DPC) [62]. If the control strategy is implemented in digital environment, it requires a high inspecting recurrence to consistently keep the controlled factors inside the hysteresis band.

2.3.3 Sliding Mode Control Technique

The sliding mode control is a propelled power converter control strategy and has a place with the group of variable structure control and versatile adaptive control [63], [64]. This control method is nonlinear in nature and well connected to linear or nonlinear frameworks. A sliding mode control strategy alongside the PWM/SVM appears in Fig. 2.7. The controller is utilized to produce the load voltage references. As the name infers, the control variable is compelled to track or slide along the predefined direction [64]. With this technique, the structure of the controller is persistently changed to accomplish a powerful and stable operation in case of the variation of the parameters and load aggravations [65].

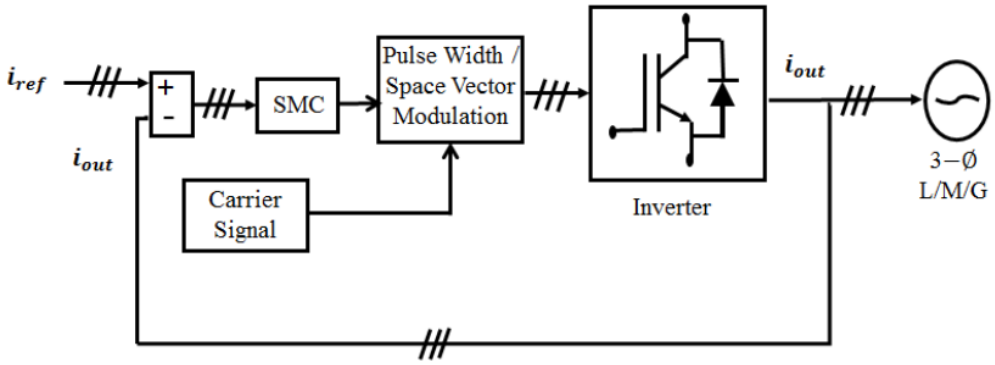


Figure 2.7: A sliding mode control strategy alongside the PWM/SVM for a three-phase load [64].

2.3.4 Artificial Intelligent based Control Techniques

The artificial neural network (ANN), genetic algorithms, and fuzzy logic controller (FLC) have found a place with the group of intelligent control methods [66]-[68]. An FLC method is showed in Fig. 2.8, where the PI controller is supplanted by the FLC. The FLC input is the error of the reference load current and the derivate of it. This controller inserts the experience, learning, and instinct of the converter administrator/planner as membership functions. Since the power converters are non-linear in nature, the strength of the system amid parameter varieties can be enhanced by utilizing the FLC without realizing the appropriate converter model. It is additionally a class of nonlinear control methods, and decidedly the best among the versatile controllers [66], [67]. The ANN speaks to the most nonexclusive type of the human reasoning procedure contrasted with the other insightful controllers [66]. The ANN-based load current direction appears in Fig. 2.9 [67]. The load current tracking error are given as inputs to the ANN through a reasonable gain or scaling factor (*K*), and the ANN controller produces changing signs to the power converter. With this methodology, a consistent switching frequency can be achieved. The upsides of FLC and ANN can be consolidated as appeared in Fig. 2.10 to accomplish better control execution [68]. Despite the fact that the intelligent controllers need not to be bother with a converter model, they require exact information about the converter operation.

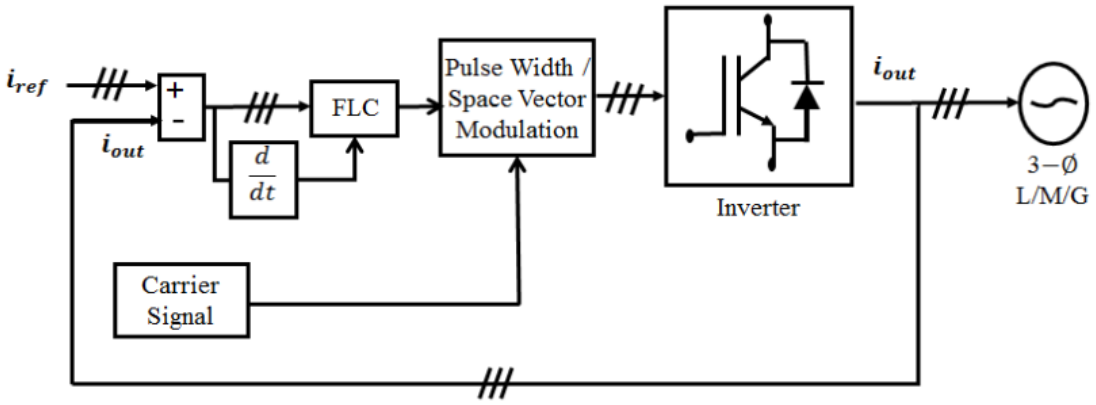


Figure 2.8: A FLC strategy utilizing the pulse width/ space vector modulation for a three-phase load [66].

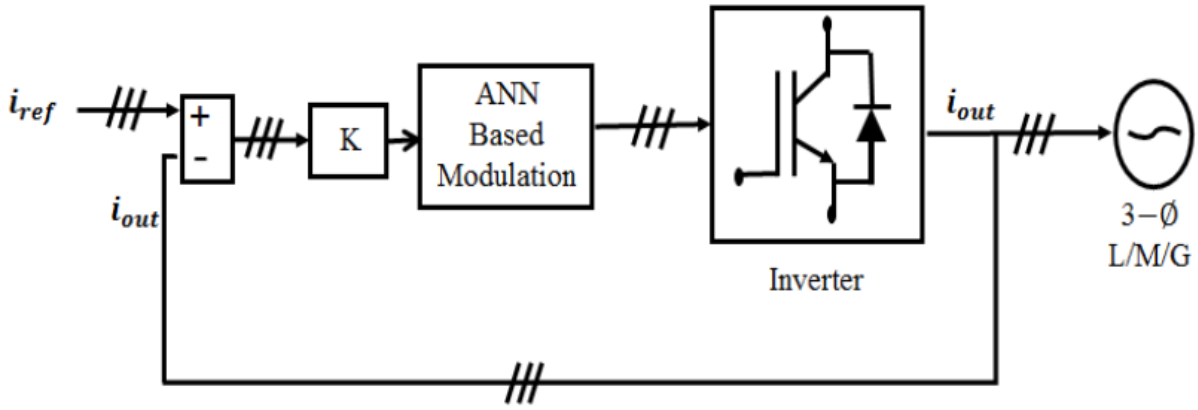


Figure 2.9: An ANN based load current controller for a three-phase load [67].

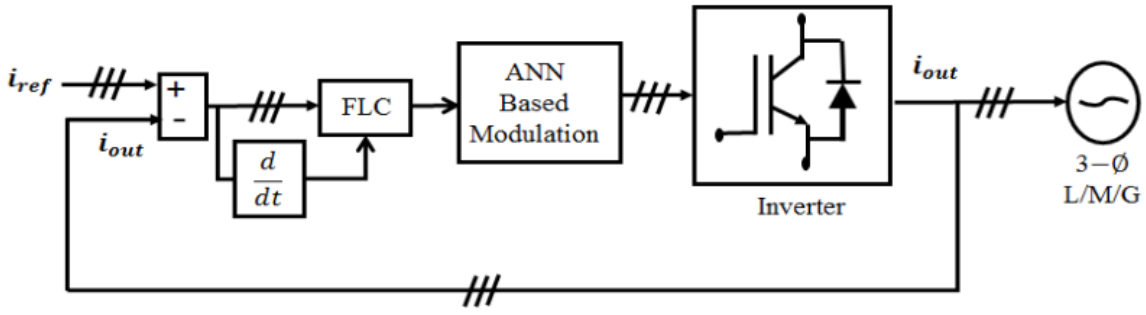


Figure 2.10: A Neuro-fuzzy controller for a three-phase load [67].

2.3.5 Model Predictive control

Model Predictive controller as shown in Fig. 2.11 provides flexibility of using any kind of algorithm that utilizes a model of the system to foresee its future behavior and chooses the most suitable control activity depending on a cost function [69]. However, the predictive control requires a high number of calculations than the classical controllers. Due to the availability of high speed microprocessors, this high number of calculations can handle with ease in a specified time frame [70].

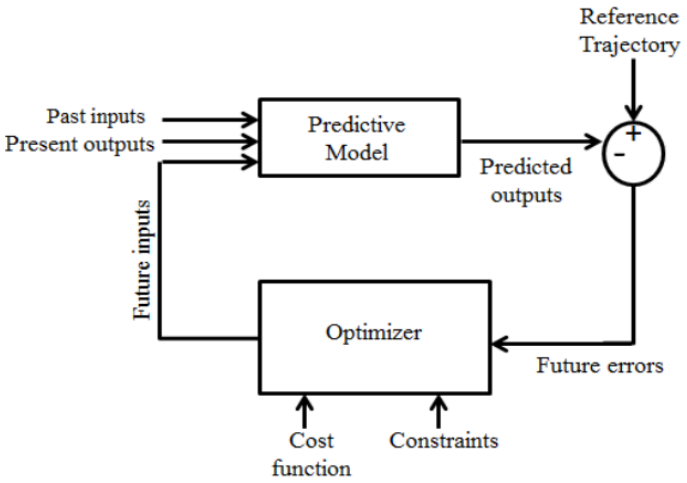


Figure 2.11: Fundamental concept of predictive control [71].

Model predictive control (MPC) is an optimization method in which a cost function is minimized for a pre-defined time horizon, subject to the system constraints and model [72]. The outcome is a succession of optimizing the cost function. Among each sampling instant, when the optimization is settled, again the controller will apply just the primary component of the succession utilizing the new estimated information and getting another sequence of optimal actuation each time.

After discussing the above control methods, it is seen that every controller has its own pros and cons. One controller may be simple but may not be accurate, again the other is accurate controllers but have some complexities. The advantages and disadvantages of the described methods are presented in Table 2.2.

Table 2.2: Pros and cons of numerous control strategies of power inverters

Control Strategy	Pros	Cons
Linear Control	• Less costly. • Simple and easily implementable. • Less complex	• Higher switching losses. • Contains lower order harmonics. • Poor power quality. • Less stable. • Higher steady-state error.
Hysteresis control	• Easily implementable. • No need of highly sophisticated technology. • No need of modulator.	• Less effective for low power applications because of the switching losses. • Switching frequency is variable as it depends on the width of the hysteresis band, load parameters, nonlinearity and operating conditions. Requires expensive filters to remove the spectral component of it.

Sliding Mode Control	• Provides robust response. • Remains stable during load disturbance and parameters variation.	• Hard to implement. • Produces high frequency oscillations. • Cannot cope up with unmatched uncertainties. • Performance depends on the sliding surface selection.
Artificial Intelligent based Controller	• Provides better performance compared to the linear controller. • Simplified controller with intelligent approach. • Provides real-time operation.	• Precise knowledge about the behavior of the converter is required. • Sufficient training data is required. • Solution results are hard to interpret.
Model Predictive Control	• Provides faster dynamics response. • Simpler in design. • Higher tracking accuracy. • Inclusion of non-linearity and constraint is possible. • Less sensitive to the system model.	• Computational complexity. • Variable switching frequency.

From Table 2.2, it can be readily said that the model predictive controller provides better performance than the other controllers. This is why predictive controller is adopted for this research work. The details about predictive controller working principle have been described in Chapter III.

Some of the features of model predictive controller which make it superior than other controllers are given below:

i) Simple concept and easily understandable.
ii) Inclusion of multiple variables constraint is possible and easier.
iii) Easy Inclusion of non-linearity in the model.
iv) Provides easier and simpler accommodation of constraints.
v) Easy implementation.
vi) Inherent discrete nature of the power converters are utilized.
vii) Many technical and control requirements can be fulfilled at the same time.
viii) Treats the power converter as a discontinuous and non-linear model which is the closest approximation to the real-time scenario.
ix) Modification of the control schemes based on the specific applications can be easily done.
x) Provides good dynamic response.
xi) Superior reference tracking accuracy.
xii) Less sensitive to the system parameters.

Apart from these superior features, MPC also faces some challenges as below [73]:

i) For selecting and estimating the proper switching state, the computational burden is higher than the other existing controllers. This complexity of the computation may be solved or mitigated by using intelligent optimization techniques.
ii) Dependency of the controller on the system architecture may decreases the quality and performance of the controller, as the controller is generally designed depending on the quality of the system model [74].
iii) Difficult to tune the parameters in the presence of constraints, sometimes much concentration should be invested on the simulation to ensure the closed loop stability.
iv) High speed processor is needed to speed up the solution time. This limitation can somehow be mitigated as high speed micro-processors are available nowadays.

The classification of MPC is shown in Fig 2.12.

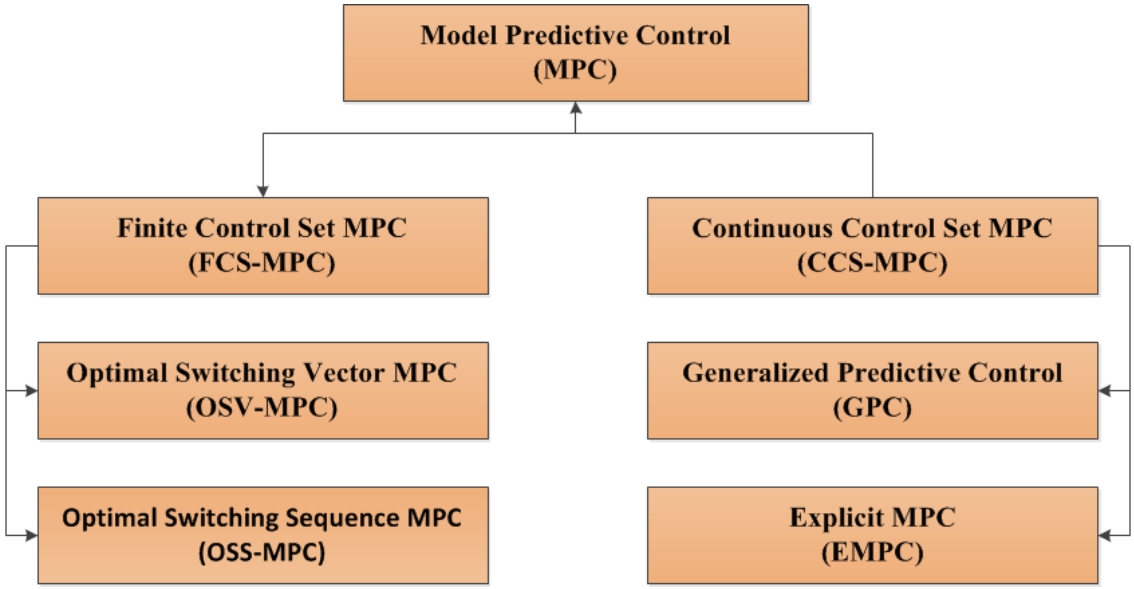


Figure 2.12: Classification of MPC strategies.

The MPC methods are broadly classified into two categories: Continuous Control Set MPC (CCS-MPC) and Finite Control Set MPC (FCS-MPC). In CCS-MPC, a continuous control signal is computed and a modulator is used to generate the desired output voltage in the power converter. The main advantage of CCS-MPC is that it produces a fixed switching frequency. The most-used CCS-MPC strategies for power electronic applications are Generalized Predictive Control (GPC) and Explicit MPC (EMPC). On other hand, FCS-MPC does not require an external modulator and it takes into account the discrete nature of the power converter to formulate the MPC algorithm. FCS-MPC can be divided into two types: Optimal Switching Vector MPC (OSV-MPC) and Optimal Switching Sequence MPC (OSS-PC). OSV-MPC is currently the most popular MPC strategy for power electronic applications. The controller is also known as FCS-MPC. It uses the possible output voltage vectors of the power converter as the control input of a system. The control objectives are predicted against every possible voltage vector. The controller reduces the optimal problem to an enumerated search algorithm. This makes the MPC strategy formulation very intuitive. The main drawbacks of OSV-MPC is that only one output voltage vector is applied during the whole switching period. Furthermore, unless an additional constraint is added, the same output voltage vector can be

used during several consecutive switching periods. Therefore, in general, it generates a variable switching frequency. OSS-MPC solves this problem by considering a control set composed of a limited number of possible switching sequences per switching period. In this way, OSS-MPC takes the time into account as an additional decision variable, i.e., the instant the switches change state, which in a way resembles a modulator in the optimization problem.

2.4 Existing Research and Current Trend of MPC

More than in last three decades, MPC becomes a popular research and development topic. In the beginning of its journey, it was mostly used in process industry. The controller could be used in power electronics applications with low switching frequency [75]. However, at that time, it was hard to adopt this strategy in power electronics because of large time required by the processor. The rapid technological advancement in the field of microprocessors brings light to solve the computational problem of MPC. As a result, MPC received more responses from the industry and became popular [76]. MPC is a strategy that is utilized for handling the dynamics of non-linear components of the system as well as various system constraints. MPC presents a sensational development in the hypothesis of recent automation technology [77]. It is widely utilized for on-grid applications as the replacement to the traditional PWM technique. Traditional PWM controller generates a significant amount of harmonic component, and a filter is utilized to remove the effect of the harmonic component [78]. Apart from on-grid application, it is deployed presently in different regions namely power electronics and drives [79], [80]. Model predictive current controller with an active damping strategy for a medium voltage drive with an LC filter is found in [81]. The strategy avoids the excitation of the filter resonance while achieving fast current control and a low switching frequency. In [82], MPC is applied for the torque regulation of a variable-speed synchronous machine fed by current source converters. A new MPC strategy called Model Predictive Pulse Pattern Control (MP3C) was presented in [83] for industrial applications with medium voltage drives. In multilevel inverter control scheme, MPC is one of the popular schemes. A number of research works have been performed in literature [18], [45], [52]. In [18], MPC based NPC has been studied where better current tracking with lower switching frequency have been achieved. MPC based back to back NPC inverter system for wind power system has been discussed in [45]. In [52], MPC based SNPC has been studied where common mode voltage has been reduced as well as neutral point balancing has been achieved.

Hence MPC is selected for controlling the current of the 3L-SNPC inverter in this research in order to observe whether this proposed topology can dominate on the conventional diode based NPC inverter.

2.5 Summary

In this chapter, different inverter topologies and their comparative analysis along with numerous control strategies for the converter are reviewed. The implementation of various control methods for the output current control is introduced alongside their pros and cons. The key features of MPC and its classification along with different flaws in it are discussed. The current trends of MPC is also discussed in the later part of this chapter.

CHAPTER III

System Modelling

3.1 Introduction

Power industries are relentlessly looking forward to ameliorating and redesigning the advanced technologies further as well as keeping pace with the future demand. Multilevel inverters play crucial role in this case as it can be deployed in different areas namely dc to ac conversion, multi-phase power supply, uninterruptible power supply, ac motor drives and so on. The main portfolio of this research is to improve the inverter system's performance. In this chapter, the construction and operation principle of the proposed three level simplified neutral point clamped inverter (3L-SNPC) and conventional three level neutral point clamped inverter (3L-NPC), block diagram of the proposed model predictive control (MPC), mathematical model, current THD improvement strategy, switching frequency reduction technique, over current protection technique, power loss analysis and execution time reduction strategy of the proposed controller are presented. It is anticipated that the power industry could easily construct the proposed model and find a sustainable solution to reduce the drawbacks of the existing inverter systems.

3.2 Proposed System Model

In this research, a finite-set MPC based three phase 3L-SNPC is proposed. MPC requires a discrete model of the system in order to achieve the control objectives. The system model includes inverter modeling, load modeling, capacitor voltage modeling and switching frequency modeling. The proposed MPC controls the load side current by means of reference tracking at each sampling time. The controller generates optimal switching state for the inverter according to a predefined cost function. The cost function is designed in such a way that it may reduce the current tracking error, maintain the neutral point voltage within an acceptable limit, protect the system from over current flow, and lessen the number of switching transition. The proposed system model is designed and analyzed in MATLAB-SIMULINK platform. The block diagram of the proposed system is shown in Fig. 3.1.

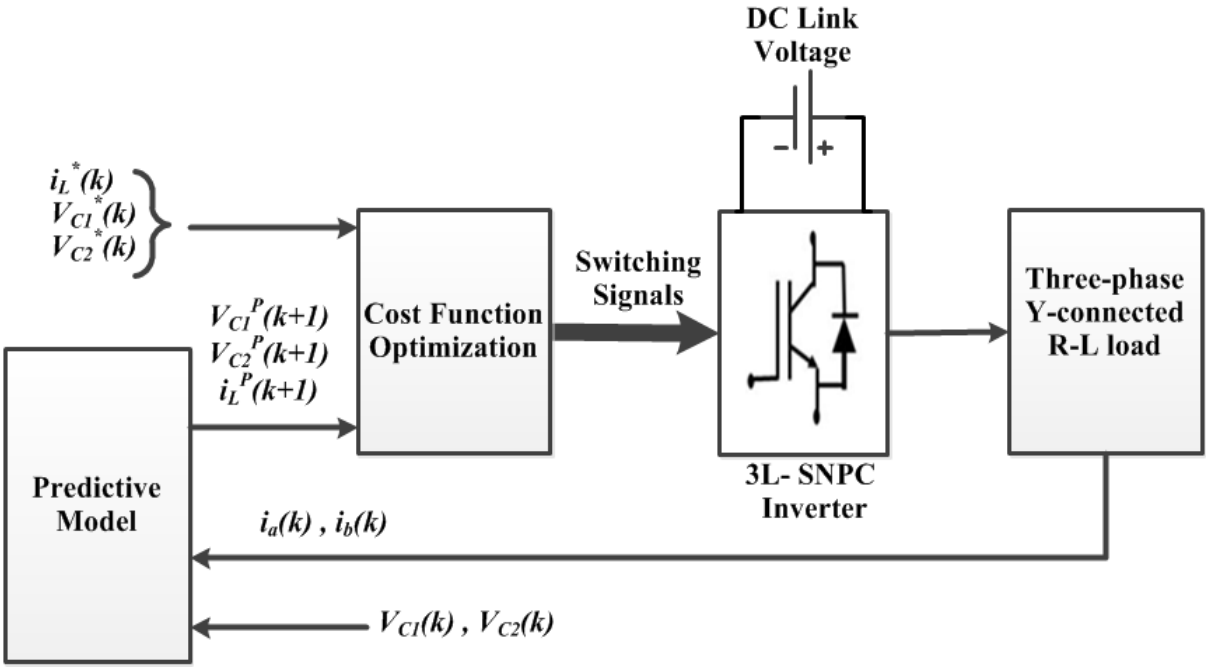


Figure 3.1: Block diagram of the proposed MPC based 3L-SNPC inverter system.

3.3 Research Methodology

The whole research work can be summarized using six different steps. The steps are given below.

- **Step 1:** Designing the proposed simplified three-level neutral point clamped inverter and the conventional three level neutral point clamped inverter.
- **Step 2:** Modeling a three phase R-L load, the neutral point voltage variation, the switching frequency and the over current protection, and then discretizing all of them for applying MPC.
- **Step 3:** Designing the proposed MPC for 3L-SNPC as well as for 3L-NPC, which is applicable for producing sinusoidal output current, maintaining the neutral point voltage variation within an acceptable limit, limiting the switching frequency and protecting the system from over current flow.
- **Step 4:** Testing the performance of the proposed 3L-SNPC inverter system in terms of steady-state and transient analysis, tracking accuracy, neutral point voltage variation, harmonic analysis, voltage stress, common mode voltage, over current protection and power loss analysis.
- **Step 5:** Comparing the performance with the existing conventional 3L-NPC.
- **Step 6:** Reducing the execution time of the proposed system by introducing voltage vector prediction based MPC and selective voltage vector based MPC schemes.

The aforementioned six steps will be discussed in more details in the following sections.

3.3.1 3L-SNPC inverter modelling

The circuit diagram of the 3L-SNPC inverter is shown in Fig. 3.2. The topology consists of a 3L dc source connected to the input of 2L inverter. The inverter is supplied by a constant DC voltage (V_{DC}), which is output of a universal bridge rectifier.

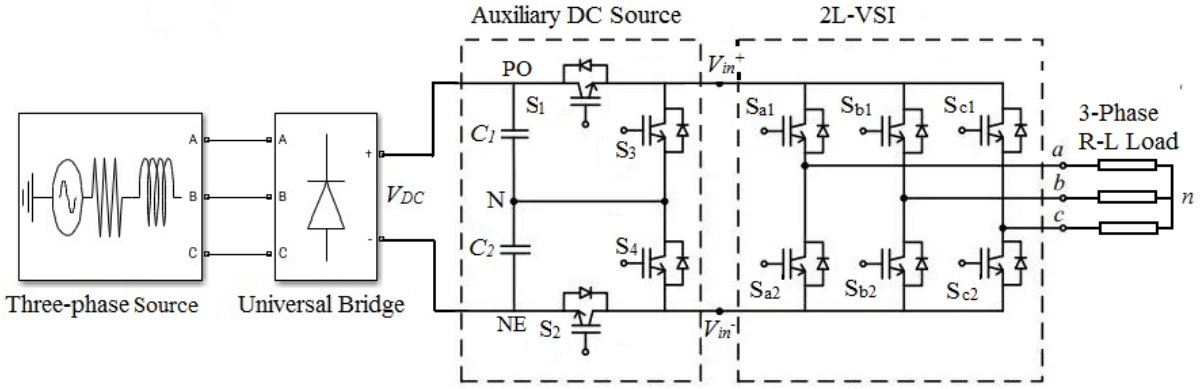


Figure 3.2: Circuit diagram of the proposed simplified 3L-NPC VSI.

The auxiliary dc source consists of two capacitors C_1 and C_2 and 4 semiconductor switches. The capacitors C_1 and C_2 are exactly equal. The PO, N and NE are symbolized the positive, neutral and negative terminals. The IGBTs S_1 – S_4 form the 3L-DC-Source with the neutral point N and are used to connect the different voltage levels to the input of the 2L-Inverter. It should be mentioned here that switches S_1 and S_3 are complementary to each other, and switches S_2 and S_4 are complementary to each other.

The 2L-VSI block consists of 6 IGBTs with anti-parallel diodes. Each arm of the VSI consists of 2 switches which are complementary to each other. A balanced three phase star connected R-L load has been deployed in the proposed system.

The steps of determining voltage vectors are shown in equations (3.1)-(3.3).

$$V_{aN} = \begin{cases} V_{DC}/2 \text{ if } S_1S_2 = 1\,0 \text{ or } 1\,1 \text{ and } S_{a1} = 1 \\ 0 \text{ if } S_1S_2 = 0\,0 \text{ and } S_{a1} = X \\ -V_{Dc}/2 \text{ if } S_1S_2 = 0\,1 \text{ or } 1\,1 \text{ and } S_{a1} = 0 \end{cases} \quad (3.1)$$

$$V_{bN} = \begin{cases} V_{DC}/2 \text{ if } S_1S_2 = 1\,0 \text{ or } 1\,1 \text{ and } S_{b1} = 1 \\ 0 \text{ if } S_1S_2 = 0\,0 \text{ and } S_{b1} = X \\ -V_{Dc}/2 \text{ if } S_1S_2 = 0\,1 \text{ or } 1\,1 \text{ and } S_{b1} = 0 \end{cases} \quad (3.2)$$

$$V_{cN} = \begin{cases} V_{DC}/2 \text{ if } S_1S_2 = 1\,0 \text{ or } 1\,1 \text{ and } S_{c1} = 1 \\ 0 \text{ if } S_1S_2 = 0\,0 \text{ and } S_{c1} = X \\ -V_{Dc}/2 \text{ if } S_1S_2 = 0\,1 \text{or } 1\,1 \text{ and } S_{c1} = 0 \end{cases} \quad (3.3)$$

where V_{DC} is the DC link voltage and X denotes don't care condition.

Considering a unit vector, $\boldsymbol{a} = e^{j2\pi/3} = -\frac{1}{2} + j\sqrt{3}/2$, which represents the phase displacement of 120^o between the phases, the output voltage vector can be defined as-

$$\boldsymbol{V} = \frac{2}{3}(V_{aN} + \boldsymbol{a}\, V_{bN} + \boldsymbol{a}^2 V_{cN}) \tag{3.4}$$

Where $V_{aN}, V_{bN}\ and\ V_{cN}$ are the phase-to-neutral (N) voltages of the inverter.
Considering all the possible combinations of the gating signals $S_1, S_2, S_{a1}, S_{b1}, S_{c1}$ there are 32 ($2^5 = 32$) possible voltage vectors, as shown in Table 3.1.

Table 3.1: Possible switching states and corresponding voltage vectors for the proposed 3L-SNPC

$\mathbf{V_n}$	Switching states					Voltage vector $\mathbf{V}=V_\alpha+jV_\beta$
	S_1	S_2	S_{a1}	S_{b1}	S_{c1}	
$\mathbf{V_1}$	1	1	1	0	0	$\frac{2}{3}V_{DC}$
$\mathbf{V_2}$	1	1	1	1	0	$\frac{1}{3}V_{DC} + j\frac{\sqrt{3}}{3}V_{DC}$
$\mathbf{V_3}$	1	1	0	1	0	$-\frac{1}{3}V_{DC} + j\frac{\sqrt{3}}{3}V_{DC}$
$\mathbf{V_4}$	1	1	0	1	1	$-\frac{2}{3}V_{DC}$
$\mathbf{V_5}$	1	1	0	0	1	$-\frac{1}{3}V_{DC} - j\frac{\sqrt{3}}{3}V_{DC}$
$\mathbf{V_6}$	1	1	1	0	1	$\frac{1}{3}V_{DC} - j\frac{\sqrt{3}}{3}V_{DC}$
$\mathbf{V_7}$	1	1	1	1	1	0
$\mathbf{V_8}$	1	1	0	0	0	0
$\mathbf{V_9}$	1	0	1	0	0	$\frac{1}{3}V_{DC}$
$\mathbf{V_{10}}$	0	1	1	0	0	$\frac{1}{3}V_{DC}$
$\mathbf{V_{11}}$	1	0	1	1	0	$\frac{1}{6}V_{DC} + j\frac{\sqrt{3}}{6}V_{DC}$
$\mathbf{V_{12}}$	0	1	1	1	0	$\frac{1}{6}V_{DC} + j\frac{\sqrt{3}}{6}V_{DC}$
$\mathbf{V_{13}}$	1	0	0	1	0	$-\frac{1}{6}V_{DC} + j\frac{\sqrt{3}}{6}V_{DC}$
$\mathbf{V_{14}}$	0	1	0	1	0	$-\frac{1}{6}V_{DC} + j\frac{\sqrt{3}}{6}V_{DC}$
$\mathbf{V_{15}}$	1	0	0	1	1	$-\frac{1}{3}V_{DC}$
$\mathbf{V_{16}}$	0	1	0	1	1	$-\frac{1}{3}V_{DC}$

V_{17}	1	0	0	0	1	$-\frac{1}{6}V_{DC} - j\frac{\sqrt{3}}{6}V_{DC}$
V_{18}	0	1	0	0	1	$-\frac{1}{6}V_{DC} - j\frac{\sqrt{3}}{6}V_{DC}$
V_{19}	1	0	1	0	1	$\frac{1}{6}V_{DC} + j\frac{\sqrt{3}}{6}V_{DC}$
V_{20}	0	1	1	0	1	$\frac{1}{6}V_{DC} + j\frac{\sqrt{3}}{6}V_{DC}$
V_{21}	1	0	1	1	1	0
V_{22}	0	1	1	1	1	0
V_{23}	1	0	0	0	0	0
V_{24}	0	1	0	0	0	0
V_{25}	0	0	1	0	0	0
V_{26}	0	0	1	1	0	0
V_{27}	0	0	0	1	0	0
V_{28}	0	0	0	1	1	0
V_{29}	0	0	0	0	1	0
V_{30}	0	0	1	0	1	0
V_{31}	0	0	1	1	1	0
V_{32}	0	0	0	0	0	0

From Table 3.1, it can be seen that 18 active vectors and 14 zero vectors are generated for the 3L-SNPC. The 32 voltage vectors can be categorized into three types: 6 Large vectors (***V_1-V_6***), 12 Small vectors (***V_9 -V_{20}***) and 14 Zero vectors (***V_7, V_8, V_{21}–V_{32}***). It should be mentioned that among 12 small vectors 6 are redundant vectors and there are in total 13 distinct voltage vectors. The 6 redundant vectors have no effect on the output load current. However, they have opposite effect on the dc-link capacitors charging and discharging. All the voltage vectors can be represented in a two-dimensional *αβ* plane as shown in Fig. 3.3. A detail description of the transformation of *abc* to *αβ* plane is presented in sub-section 3.3.2.

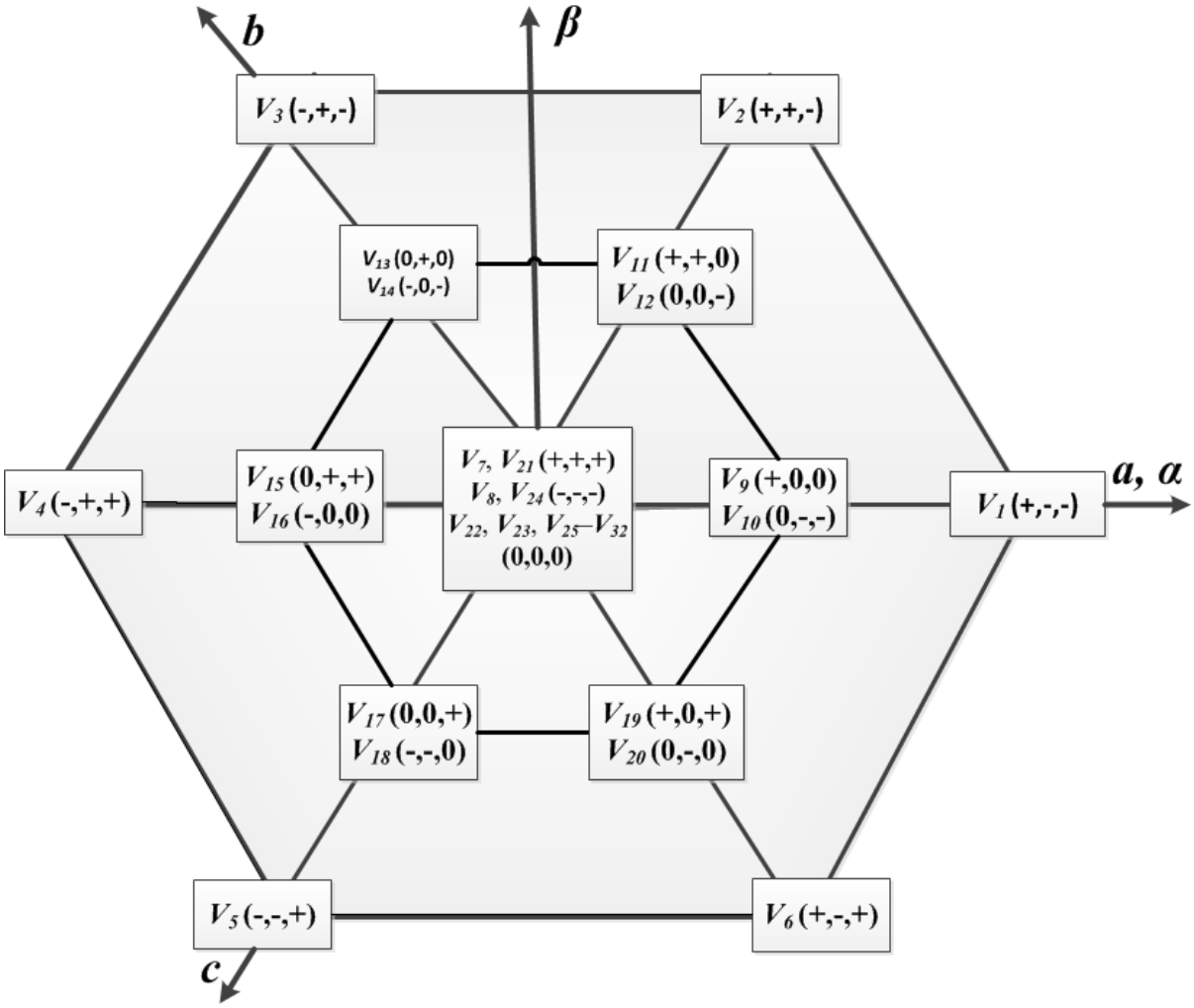


Figure 3.3: Space distribution of all possible voltage vectors of the proposed 3L-SNPC.

3.3.2 *a-b-c* to *αβ* coordinate transformation

In order to make easy the control configuration procedure of a three-phase system, two fundamental coordinate transformations are utilized: Clarke transformation (*abc* to *αβ*) and Park transformation (*abc* to *dq*) transformation. In this study, the Clarke (αβ) transformation is used to analyze the system's performance.

In *αβ* transformations, the dimension of the state-space representation of the three phase system is reduced. The expressions related to this transformation is [84].

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_\gamma \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{3.5}$$

where, the three-phase output voltage is represented by V_a, V_b and V_c. In a three-phase symmetrical system, where $V_a + V_b + V_c = 0$ and V_γ=0, only two vectors V_α and V_β can represent the three-phase system. In another sense, γ axis is basically orthogonal to $\alpha\beta$ plane and no projection exists due to γ axis on the plane. Therefore, the transformations of $\alpha\beta\gamma$ can

be called as $\alpha\beta$ transformations. It should be mentioned that this *abc* to $\alpha\beta$ conversion is equally applicable to three phase currents and powers.

Moreover, the inverse transformation of transformations can be expressed as [84].

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{3.6}$$

Therefore, under symmetrical condition, this transformation can convert the two phase stationary system to the three phase symmetrical system.

Since the measured currents and the reference currents both are the three-phase variables, this transformations are applied to both of the two variables. The graphical representation and the MATLAB implementation of the $\alpha\beta$ transformation are shown in Fig. 3.4.

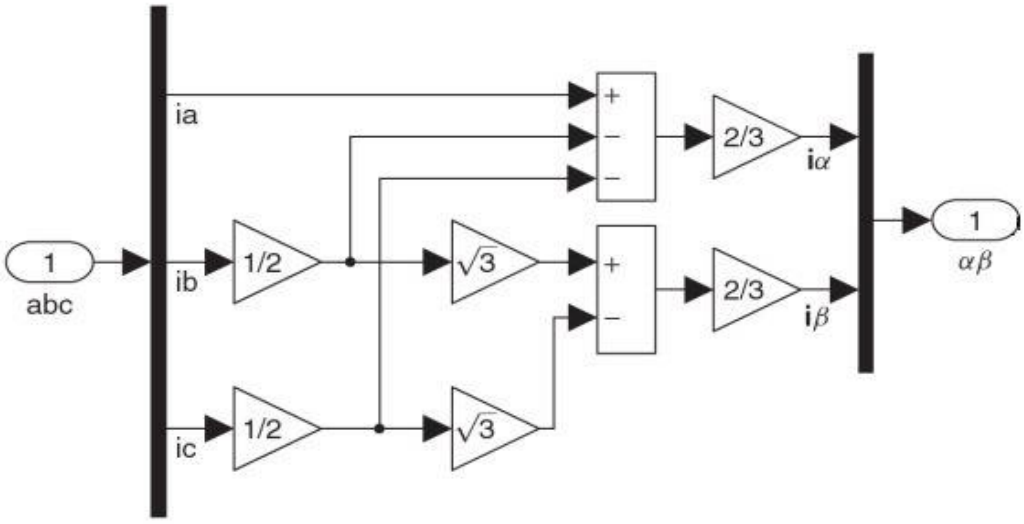


Figure 3.4: MATLAB implementation of the *abc* to $\alpha\beta$ transformation.

3.3.3 Conventional 3L-NPC

The circuit diagram of the conventional 3L-NPC inverter is shown in Fig. 3.5. From Fig. 3.5, it is observed that there are 4 IGBTs with anti-parallel diodes in each phase. The dc link side consists of two same capacitors of C_1 and C_2.

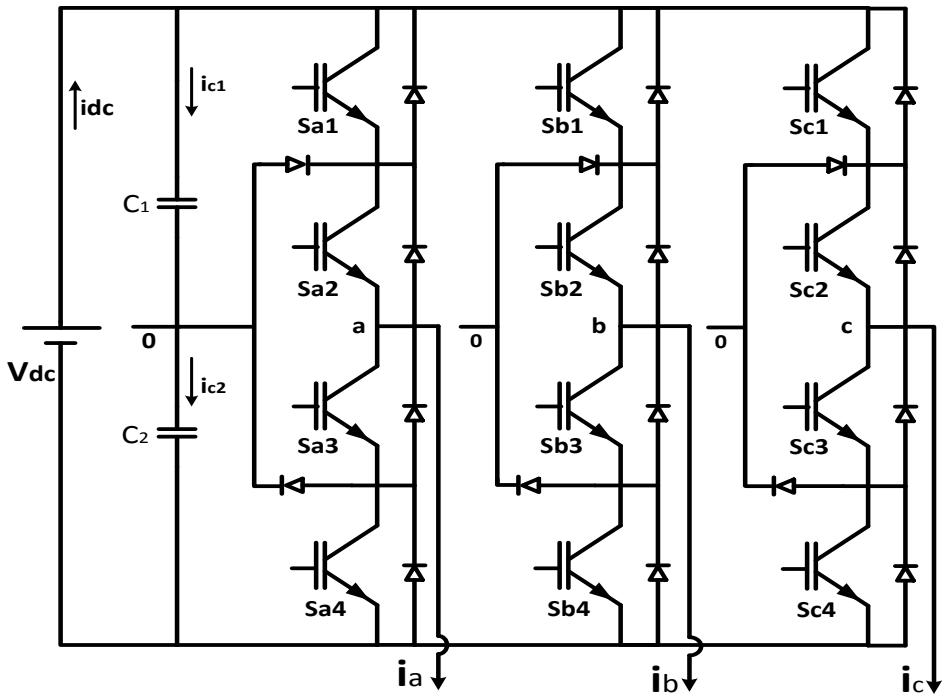


Figure 3.5: Circuit diagram of the conventional 3L-NPC VSI.

The capacitors are so chosen that the voltage drop across them will be equal. Three phase star connected R-L load is connected at the output terminals of the inverter.

The steps of determining voltage vectors are shown in equations (3.7)-(3.10).

$$V_{aN} = \begin{cases} {}^{V_{dc}}/_{2} \text{ if } S_{a1}S_{a2} = 1\ 1 \\ 0 \text{ if } S_{a2}S_{a3} = 1\ 1 \\ -{}^{V_{dc}}/_{2} \text{ if } S_{a1}S_{a2} = 0\ 0 \end{cases} \tag{3.7}$$

$$V_{bN} = \begin{cases} {}^{V_{dc}}/_{2} \text{ if } S_{b1}S_{b2} = 1\ 1 \\ 0 \text{ if } S_{b2}S_{b3} = 1\ 1 \\ -{}^{V_{dc}}/_{2} \text{ if } S_{b1}S_{b2} = 0\ 0 \end{cases} \tag{3.8}$$

$$V_{cN} = \begin{cases} {}^{V_{dc}}/_{2} \text{ if } S_{c1}S_{c2} = 1\ 1 \\ 0 \text{ if } S_{c2}S_{c3} = 0\ 0 \\ -{}^{V_{dc}}/_{2} \text{ if } S_{c1}S_{c2} = 0\ 0 \end{cases} \tag{3.9}$$

The output voltage vector can be defined as-

$$\boldsymbol{V} = \frac{2}{3}(V_{aN} + \boldsymbol{a}V_{bN} + \boldsymbol{a}^2 V_{cN}) \tag{3.10}$$

where, $\boldsymbol{a} = e^{j2\pi/3}$.

Considering all the possible combinations of the gate signals S_{a1}, S_{a2}, S_{b1}, S_{b2}, S_{c1} and S_{c2}, corresponding 27 voltage vectors are obtained which is shown in Table 3.2.

$\mathbf{V_n}$	Switching states						Voltage vector $\mathbf{V}=V_\alpha+jV_\beta$
	S_{a1}	S_{a2}	S_{b1}	S_{b2}	S_{c1}	S_{c2}	
$\mathbf{V_1}$	0	0	0	0	0	0	0
$\mathbf{V_2}$	0	1	0	1	0	1	0
$\mathbf{V_3}$	1	1	1	1	1	1	0
$\mathbf{V_4}$	1	1	0	1	0	1	$\frac{1}{3}V_{DC}$
$\mathbf{V_5}$	0	1	0	0	0	0	$\frac{1}{3}V_{DC}$
$\mathbf{V_6}$	1	1	1	1	0	1	$\frac{1}{6}V_{DC}+j\frac{\sqrt{3}}{6}V_{DC}$
$\mathbf{V_7}$	0	1	0	1	0	0	$\frac{1}{6}V_{DC}+j\frac{\sqrt{3}}{6}V_{DC}$
$\mathbf{V_8}$	0	1	1	1	0	1	$-\frac{1}{6}V_{DC}+j\frac{\sqrt{3}}{6}V_{DC}$
$\mathbf{V_9}$	0	0	0	1	0	0	$-\frac{1}{6}V_{DC}+j\frac{\sqrt{3}}{6}V_{DC}$
$\mathbf{V_{10}}$	0	1	1	1	1	1	$-\frac{1}{3}V_{DC}$
$\mathbf{V_{11}}$	0	0	0	1	0	1	$-\frac{1}{3}V_{DC}$
$\mathbf{V_{12}}$	0	1	0	1	1	1	$-\frac{1}{6}V_{DC}-j\frac{\sqrt{3}}{6}V_{DC}$
$\mathbf{V_{13}}$	0	0	0	0	0	1	$-\frac{1}{6}V_{DC}-j\frac{\sqrt{3}}{6}V_{DC}$
$\mathbf{V_{14}}$	1	1	0	1	1	1	$\frac{1}{6}V_{DC}-j\frac{\sqrt{3}}{6}V_{DC}$
$\mathbf{V_{15}}$	0	1	0	0	0	1	$\frac{1}{6}V_{DC}-j\frac{\sqrt{3}}{6}V_{DC}$
$\mathbf{V_{16}}$	1	1	0	1	0	1	$\frac{1}{2}V_{DC}+j\frac{\sqrt{3}}{6}V_{DC}$
$\mathbf{V_{17}}$	0	0	1	1	0	1	$j\frac{1}{\sqrt{3}}V_{DC}$
$\mathbf{V_{18}}$	0	0	1	1	0	1	$-\frac{1}{2}V_{DC}+j\frac{\sqrt{3}}{6}V_{DC}$
$\mathbf{V_{19}}$	0	0	0	1	1	1	$-\frac{1}{2}V_{DC}-j\frac{\sqrt{3}}{6}V_{DC}$
$\mathbf{V_{20}}$	0	1	0	0	1	1	$-j\frac{1}{\sqrt{3}}V_{DC}$
$\mathbf{V_{21}}$	1	1	0	0	0	1	$\frac{1}{2}V_{DC}-j\frac{\sqrt{3}}{6}V_{DC}$
$\mathbf{V_{22}}$	1	1	0	0	0	0	$\frac{2}{3}V_{DC}$

V_{23}	1	1	1	1	0	0	$\frac{1}{3}V_{DC} + j\frac{\sqrt{3}}{3}V_{DC}$
V_{24}	0	0	1	1	0	0	$-\frac{1}{3}V_{DC} + j\frac{\sqrt{3}}{3}V_{DC}$
V_{25}	0	0	1	1	1	1	$-\frac{2}{3}V_{DC}$
V_{26}	0	0	0	0	1	1	$-\frac{1}{3}V_{DC} - j\frac{\sqrt{3}}{3}V_{DC}$
V_{27}	1	1	0	0	1	1	$\frac{1}{3}V_{DC} - j\frac{\sqrt{3}}{3}V_{DC}$

The space vector diagram of the 3L-NPC is shown in Fig. 3.6.

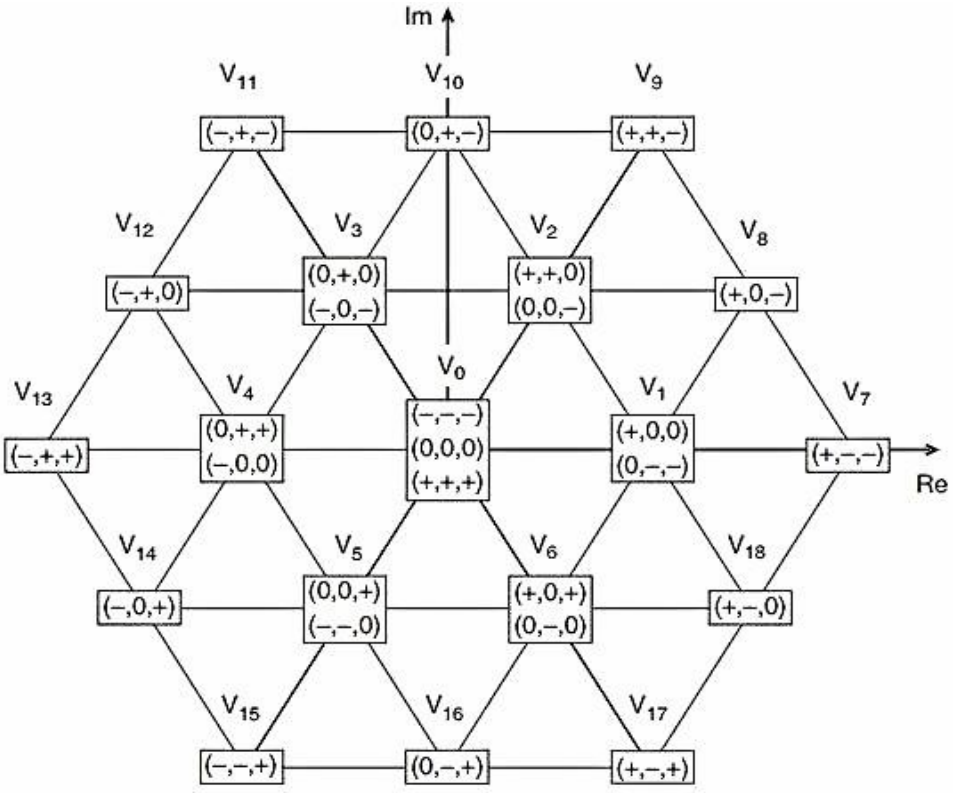


Figure 3.6: Space distribution of all the possible voltage vectors of the 3L-NPC [73].

There are four categories of voltage vectors: 6 large vectors (***V_7, V_9, V_{11}, V_{13}, V_{15}, V_{17}***), 6 medium vectors (***V_8, V_{10}, V_{12}, V_{14}, V_{16}, V_{18}***), 12 small vectors (***V_1-V_6***) in which six are redundant and 3 zero vectors (***V_0***).

3.3.4 Three phase load model

Load modeling is necessary after designing the converter model. The three-phase voltage (v_{aN}, v_{bN}, v_{cN}) of both simplified and conventional NPC can be expressed as-

$$v_{aN} = L\frac{di_a}{dt} + Ri_a + e_a + v_{nN} \tag{3.11}$$

$$v_{bN} = L\frac{di_b}{dt} + Ri_b + e_b + v_{nN} \tag{3.12}$$

$$v_{cN} = L\frac{di_c}{dt} + Ri_c + e_c + v_{nN} \tag{3.13}$$

where, the resistance and inductance of the load are indicated by *R* and *L*. The output voltage vector can be presented as

$$\boldsymbol{v} = \frac{2}{3}(v_{aN} + \boldsymbol{a}\, v_{bN} + \boldsymbol{a^2} v_{cN}) \tag{3.14}$$

By substituting (3.11)-(3.13) into (3.14), the load current dynamics can be obtained as:

$$v = L\frac{d}{dt}\left(\frac{2}{3}(i_a + \boldsymbol{a}i_b + \boldsymbol{a^2}i_c)\right) + R\left(\frac{2}{3}(i_a + ai_b + a^2 i_c)\right) + \frac{2}{3}(e_a + \boldsymbol{a}e_b + \boldsymbol{a^2}e_c) + \frac{2}{3}(v_{nN} + \boldsymbol{a}v_{nN} + \boldsymbol{a^2}v_{nN}) \tag{3.15}$$

Since the proposed has been considered RL load, back emf, *e* is set to 0

The load current, *i* equations are respectively-

$$i = \frac{2}{3}(i_a + \boldsymbol{a}i_b + \boldsymbol{a^2}i_c) \tag{3.16}$$

Since the term $\frac{2}{3}(v_{nN} + \boldsymbol{a}v_{nN} + \boldsymbol{a}^2 v_{nN}) = \frac{2}{3}v_{nN}(1 + \boldsymbol{a} + \boldsymbol{a}^2) = 0$, substituting eqn. (3.16) in eqn. (3.15) the voltage expression can be written as

$$v = Ri + L\frac{d\boldsymbol{i}}{dt} \tag{3.17}$$

However, a discrete load model is required for the MPC.

3.3.5 Discrete-time model for prediction

The proposed model predictive control is actually an optimization algorithm. To actualize this algorithm on digital platform, the continuous time model ought to be changed over to discrete time. In the control hypothesis, numerous discretization strategies are accessible, for example, forward difference, backward difference, bilinear transformations, impulse-invariant and zero-order hold. Because of the first order nature of the state equations that depicts in Eqn. (3.18), a first-order approximation for the derivative can be obtained by forward or backward Euler method [85].

Let us consider a first-order general differential equation

$$\frac{dx}{dt} = Ax(k) + Bu(k) \tag{3.18}$$

Now considering the present and future samples *k* and *(k+1),* the forward Euler technique can be expressed as-

$$\frac{dx}{dt} = \frac{x(k+1) - x(k)}{T_s} \tag{3.19}$$

where, T_s presents the discrete sampling time.

By replacing (3.19) into (3.18), the discrete-time model for the control variable *x* can be expressed as-

$$\frac{x(k+1) - x(k)}{T_s} = Ax(k) + Bu(k) \tag{3.20}$$

$$x(k+1) = (1 + AT_s)x(k) + BT_s u(k) \tag{3.21}$$

If the present and past samples are k and k-1 respectively, the approximation for the derivative using backward Euler method can be expressed as-

$$\frac{dx}{dt} = \frac{x(k)-x(k-1)}{T_s} \tag{3.22}$$

The expression from (3.22) can also be replaced to (3.18) and can be expressed as-

$$x(k) = \frac{x(k-1)}{(1-AT_s)} + \frac{BT_s u(k)}{(1-AT_s)} \tag{3.23}$$

In this study the control variable '*x*' in (3.19) would be load current and capacitor voltage dynamics.

3.3.6 Load current prediction

The forward Euler method is utilized in this study for the discretization of load current. Hence, the load current derivative $\frac{d\boldsymbol{i}}{dt}$ is put in place of $\frac{dx}{dt}$ in (3.18) the forward Euler approximation can be expressed as-

$$\frac{d\boldsymbol{i}}{dt} \approx \frac{\boldsymbol{i}(k+1)-\boldsymbol{i}(k)}{T_s} \tag{3.24}$$

Now substitute (3.24) in Eqn. (3.17) in order to obtain the future load current at instant (*k* + 1) as [73]-

$$\mathrm{i^p(k+1)} = \left(1\text{-}\frac{\mathrm{RT_s}}{\mathrm{L}}\right)\mathrm{i(k)} + \frac{\mathrm{T_s}}{\mathrm{L}}\left(\mathrm{v(k)}\right) \tag{3.25}$$

The superscript p denotes the predicted variables. Where, $\boldsymbol{i^p}(k+1)$ denotes predicted load current.

3.3.7 Neutral point voltage prediction

Capacitor voltage balancing is one of the crucial factors for NPC inverter. It is because unbalanced capacitor voltages introduce neutral-point voltage variation and thus ripple in output current. The neutral point voltage is zero for two balanced capacitor voltages. Both the proposed simplified and the conventional NPC require neutral point voltage balancing. Similar to the load current prediction, the forward Euler approximation is used to predict capacitor voltages-

$$\frac{dv_c}{dt} \approx \frac{v_c(k+1)-v_c(k)}{T_s} \tag{3.26}$$

Here, T_s is the sampling time. From (3.26) the following capacitor voltages in discrete time can be expressed as [73]-

$$\boldsymbol{v}_{c1}^{p}(k+1) = \boldsymbol{v}_{c1}(k) + \frac{1}{C}\boldsymbol{i}_{c1}(k)T_s \tag{3.27}$$

$$\boldsymbol{v}_{c2}^{p}(k+1) = \boldsymbol{v}_{c2}(k) + \frac{1}{C}\boldsymbol{i}_{c2}(k)T_s \tag{3.28}$$

Where, $\boldsymbol{v}_{c1}(k)$ and $\boldsymbol{v}_{c2}(k)$ are the measured capacitor voltages. *C* is the capacitance of each capacitor, $\boldsymbol{i}_{c1}(k)$ and $\boldsymbol{i}_{c2}(k)$ are the currents flowing through the capacitors.

Now by subtracting (3.27) from (3.28) we can calculate the neutral point voltage. The expression of neutral point voltage is-

$$\boldsymbol{dv}_{c12}^{p}(k+1) = [\boldsymbol{v}_{c2}(k) - \boldsymbol{v}_{c2}(k)] + \frac{1}{C}T_s[\boldsymbol{i}_{c2}(k) - \boldsymbol{i}_{c1}(k)] \tag{3.29}$$

The voltage variation $\boldsymbol{dv}_{c12}^{p}(k+1)$ is used in the cost function of MPC minimizing the neutral point voltage variation.

3.3.8 Average switching frequency reduction

The switching frequency is directly related to the switching loss of the inverter. In order to reduce the switching frequency, a number of commutations, n_{sw} of the semiconductor devices is included in the cost function with a weighting factor λ_{sw}. The expression of n_{sw} is shown in 3.30.

$$n_{sw}(k+1) = \sum_{ns} |S_{ns}(k+1)_i - S_{ns}(k)| \tag{3.30}$$

where, the possible switching state for the next sample instant (k+1) is represented by$S_{ns}(k+1)$, the applied switching state to the inverter at time is indicated by S_{ns}(k) and *i* is the index of voltage vectors so the value of *i* will be 1-32 for SNPC and 1-27 for NPC. The subscript notation '*ns*' indicates the number of switches considered for average switching frequency calculation which is 10 for SNPC and 12 for NPC.

The average switching frequency f_{sw} per semiconductor switch is calculated by (3.31) considering the total number of switching transitions $n_{sw}(T)$ over the duration *T*.

$$f_{sw} = n_{sw}(T)/\mathrm{N/T} \tag{3.31}$$

Where, N is the total number of switching devices which is 12 for NPC and 10 for SNPC.

3.3.9 Over-current protection

The over current protection is implemented by using a simple control statement in the algorithm. The value of the predicted currents corresponding to the possible switching states in each sampling period is monitored. If the current exceeds a predefined value then the cost function shows very high value by considering a constraint λ_{ocp} in it to neglect that particular switching states and thus protects the system from over-current. If the predicted current is less than the predefined value, the cost function does not consider it by setting the λ_{ocp} as zero. The flow chart of this constraint is shown in Fig. 3.7.

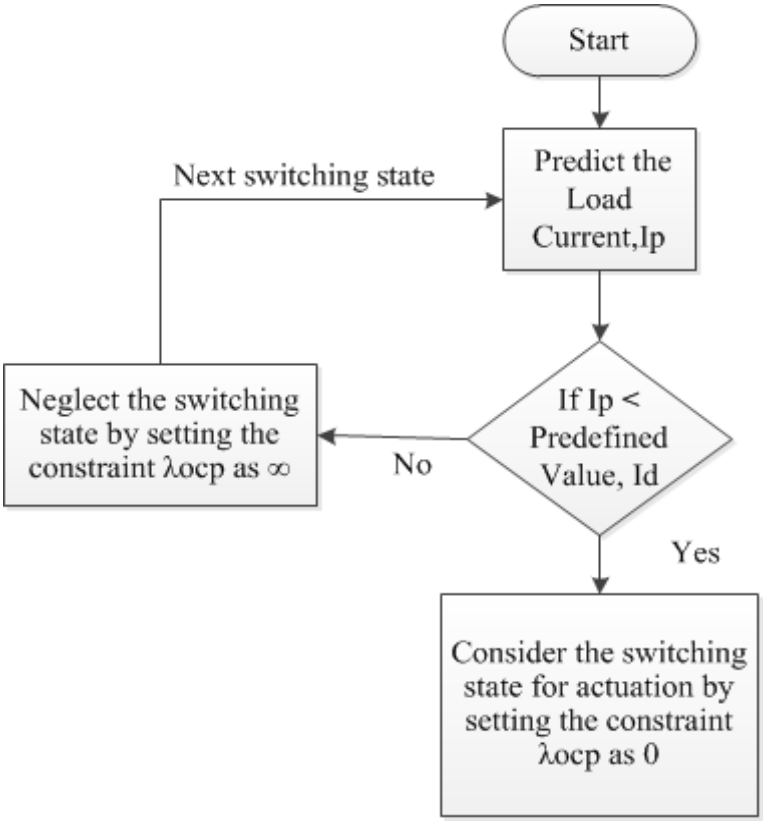


Figure 3.7: Flow chart of over-current protection feature.

3.3.10 Control parameter flexibility in MPC

For the design of a MPC, the most significant parameters is the design of the cost function, as it not only permits the proper selection of control objectives of the specific application but also provides the flexibility of adding any other constraints to it. This distinctive feature allows controlling various controlling parameters such as voltage, current, and active and reactive power by utilizing a single cost function. The various controlling parameters that can be added to a single cost functions are presented in Fig. 3.8.

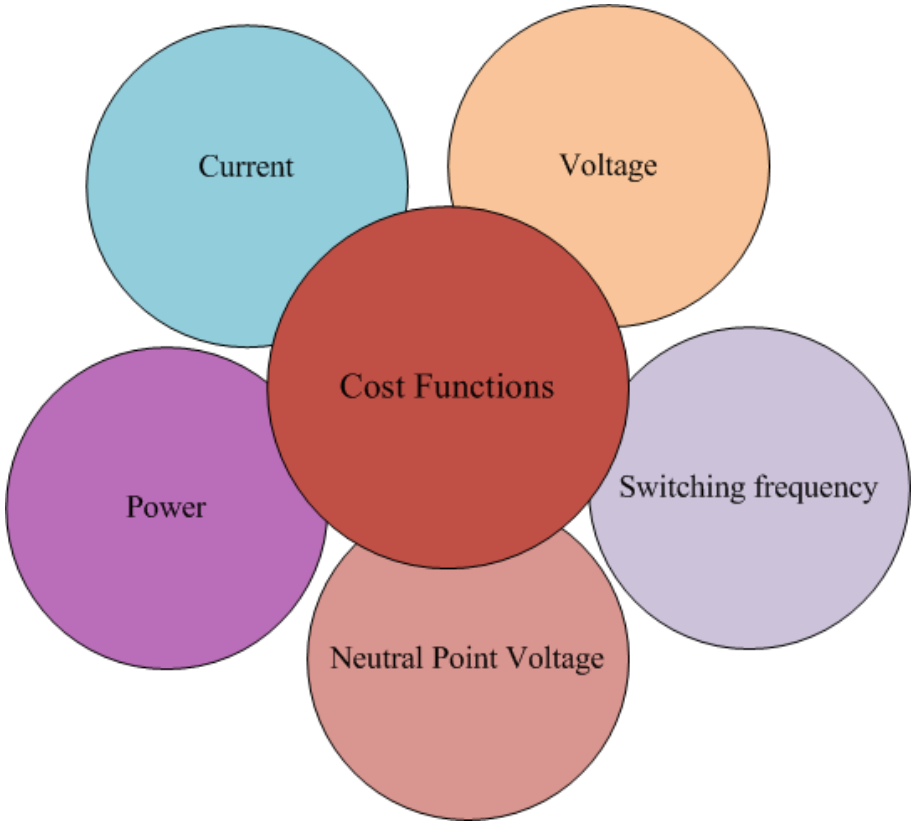


Figure 3.8: Control parameter flexibility of MPC.

From Fig. 3.8, it can be seen that because of the cost function flexibility of the proposed MPC, different control parameters with different units can be added to a single cost function. This addition of each term with different magnitudes and units is done by multiplying them with different weighting factors. The weighting factors also set priority of one control variable over another control variable. However, the choice of the weighting factors is not straight forward [17]. A few exact ways to deal with a fix weight factor utilizing experimentation have been researched in the literature [17]. However, a settled weight factor is not powerful to parameter variation and different vulnerabilities of the system. The generalized formulation of adding different constraints with weight factor can be expressed as-

$$g = \lambda_1\left[x_1^p(k+1) - x_1^*(k+1)\right] + \lambda_2\left[x_2^p(k+1) - x_2^*(k+1)\right] + \lambda_3\left[x_3^p(k+1) - x_3^*(k+1)\right] + \cdots\cdots + \lambda_n[x_n^p(k+1) - x_n^*(k+1)] \quad (3.32)$$

where, the weighting factors are presented by $\lambda_{1\ldots n}$ for each controlling parameter, p and * represent the predictive and reference components. All the possible control actions are evaluated against the control objectives. Using the cost function, the control action which yields minimum cost, is stored and applied to the inverter for the next sampling instant.

The cost function for the proposed inverter system is composed of current tracking error, capacitor voltage balancing, over-current protection, average switching frequency reduction and is shown in Eqn. 3.33.

$$g = \lambda_i\left[i_L^p(k+1) - i_L^*(k+1)\right] + \lambda_{npv}\left[dvc_{12}^p(k+1) - dvc_{12}^*(k+1)\right] + \lambda_{sw}[n_{sw}] + \lambda_{ocp} \quad (3.33)$$

Where, $\lambda_i, \lambda_{npv}, \lambda_{sw}$ and λ_{ocp} are the weighting factor for current tracking error, neutral-point voltage variation, average switching frequency reduction and variable term for over-current protection, respectively. n_{sw} is the number of commutations of the power semiconductor devices. It should be mentioned here that the weighting factor basically denotes the priority of each constraint. The higher the value of weighting factor the more prior will be given to that constraint. Hence, proper selection of weighting factor is badly required for smooth operation of the controller. The selection of weighting factor and its impact is discussed in more details in chapter IV.

3.3.11 Algorithm of the proposed MPC

The MPC algorithm consists of four sections: (i) measurement, (ii) prediction, (iii) optimization, and (iv) application of the optimal switching states, x_{opt}. For the proposed simplified 3L-NPC, the load currents and capacitor voltages are measured. Then, all the control objectives, such as load current, neutral point voltage variation, number of switching transition and over current protection, are predicted against 32 possible voltage vectors. An optimal voltage vector is selected by minimizing a predefined cost function as explained in sub-section 3.3.9. Finally, the optimal voltage vector is applied to the load terminals through the inverter. The overall control strategy is executed using the following steps.

Step 1: The load current i(k), capacitor voltages $V_{c1}(k)$ and $V_{c2}(k)$ are measured.
Step 2: For the immediate next sampling instant, the future load current $i_L^p(k+1)$, neutral point voltage variation $dvc_{12}^p(k+1)$ and number of switching transitions n_{sw} are predicted for all the possible switching states. Here $i_L^p(k+1)$ is also compared with maximum current limit which is predefined to protect the system from over-current.
Step 3: The predicted control objectives are evaluated by minimizing the cost function g.
Step 4: For the minimized cost function, the optimal switching state is selected.
Step 5: The selected switching state x_{opt} is then applied to the next sampling instant.

The control algorithm is further illustrated by using a flow chart and shown in Fig. 3.9. It can be seen that there are two loops: inner and outer. The inner loop is executed for each possible voltage vector, and the outer loop is executed for every sampling time in order to determine the optimal switching state. The equations and the cost function used in the flow chart are detailed in previous sub-sections. In Fig. 3.9, N_V indicates the total number of voltage vectors which should be 32 for the proposed SNPC inverter topology and 27 for the conventional NPC inverter topology. The working strategy of the algorithm is presented in the next sub-section.

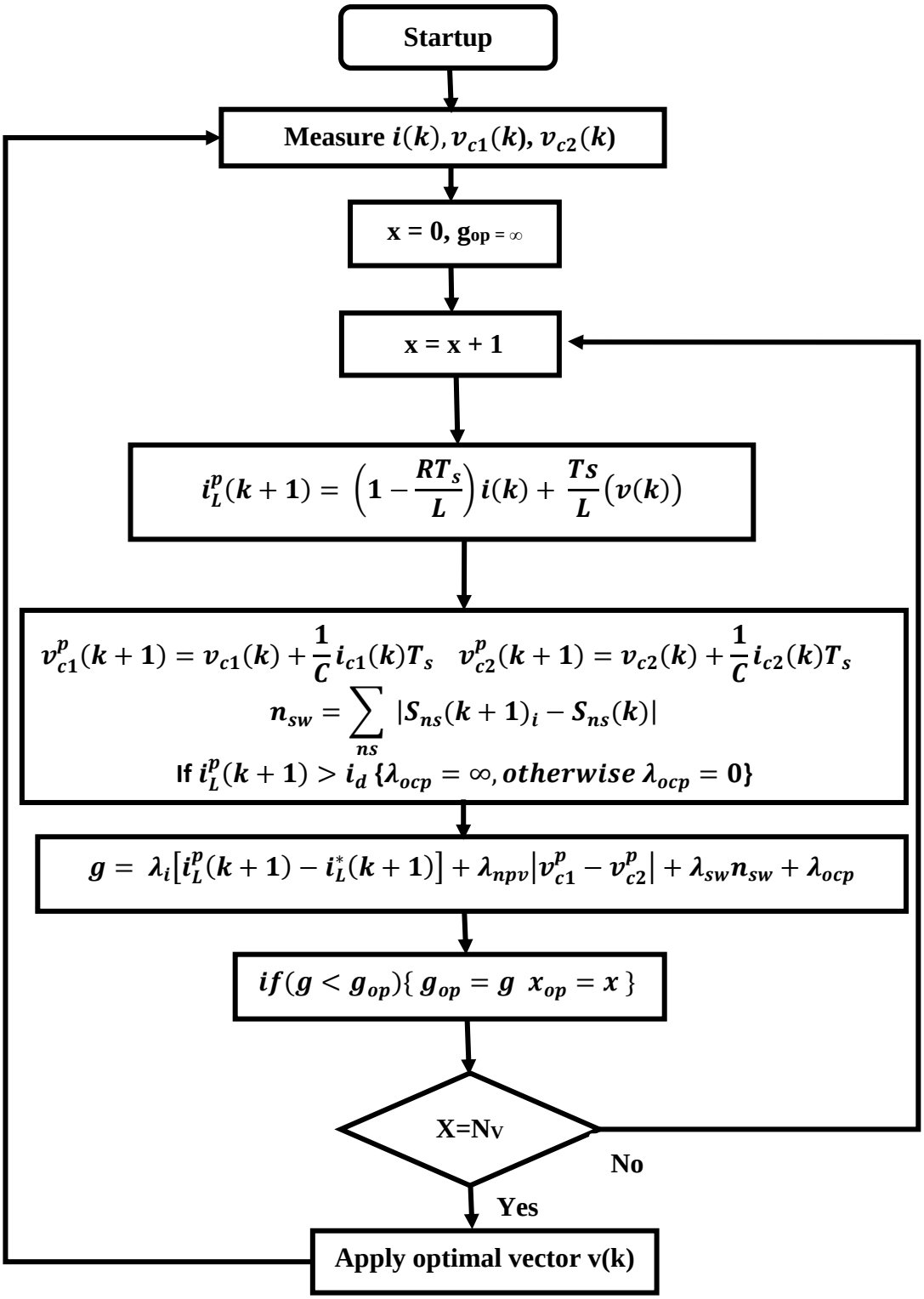


Figure 3.9: Flow chart of the proposed predictive controller.

3.3.12 Working strategy of the proposed MPC

For demonstrating the working strategy of the proposed MPC, a pictorial representation is presented in Figs. 3.10, 3.11 and 3.12. For easy understanding, the principle of MPC is explained for a two-level VSI where only eight voltage vectors are present. The three-phase load currents and their references are presented in the figures after the transformation of *abc*

frame to $\alpha\beta$ plane. The future predictive load currents $i_L(k+1)$ are evaluated by utilizing the measured current $i(k)$ for all the available switching voltage vector $v(k)$, which is indicated as $i_p(k+1)$ in Fig. 3.10. It is seen that the vector V2 chooses the nearest predicted current vector to the reference. Moreover, from Fig. 3.11, for the load current (i_α), the minimal error is provided by vectors V_2 and V_6. From Fig. 3.12, for the load current (i_β), the minimal error is provided by the vectors V_2 and V_3. Therefore, the vectors V_2 is selected as the optimal vector which provides the most optimized cost function. Hence, it can be said that the difference between the predicted and reference vector characterizes the cost function as presented in figures 3.10-3.12. Although for current control, it is easier to visualize these errors, for complicated cost function, this representation will be too difficult. In the proposed system, apart from current, voltage balancing, average switching frequency reduction, over-current protection these are also added to the cost function. In that case, the controller chooses that switching states as well as voltage vector which reduces the overall cost function g value.

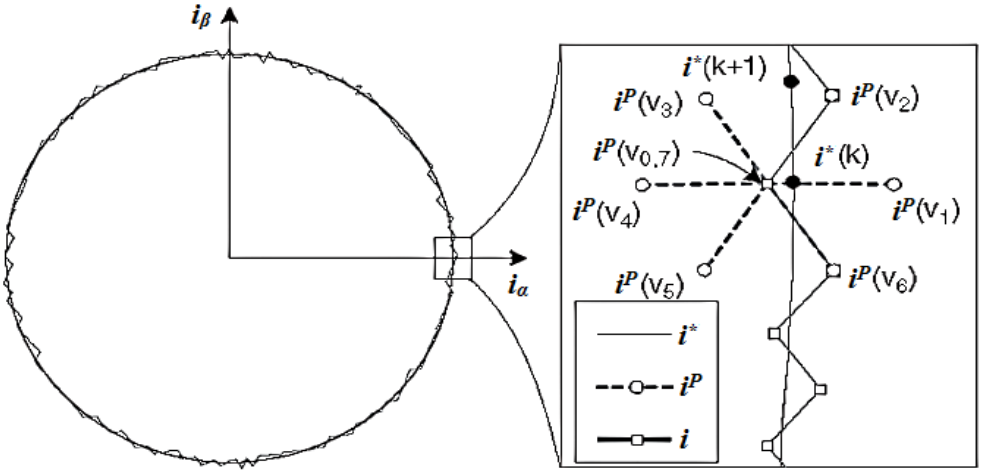


Figure 3.10: The representation of reference and predictive currents in vector plot [73].

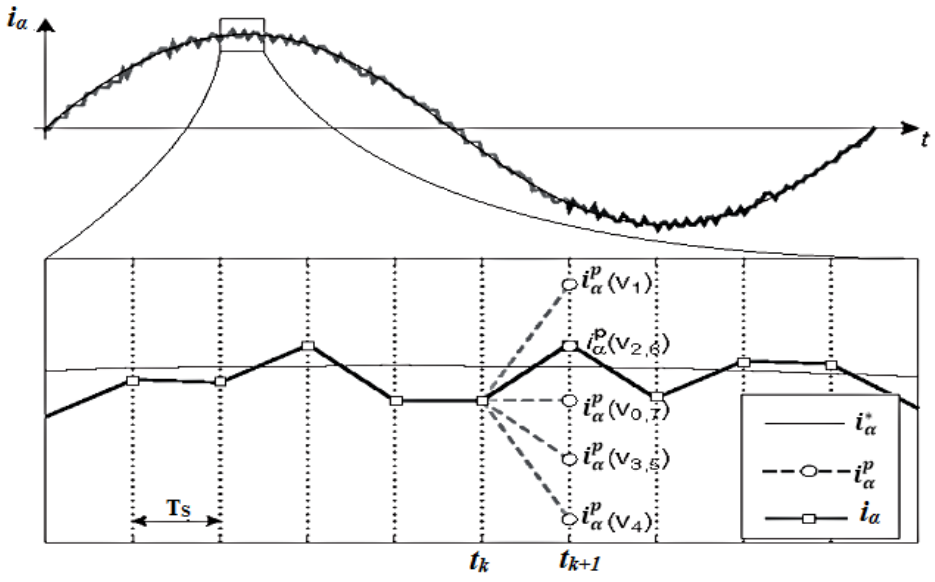


Figure 3.11: Graphical representation of selecting optimal voltage vectors of reference and predicted currents of i_α [73].

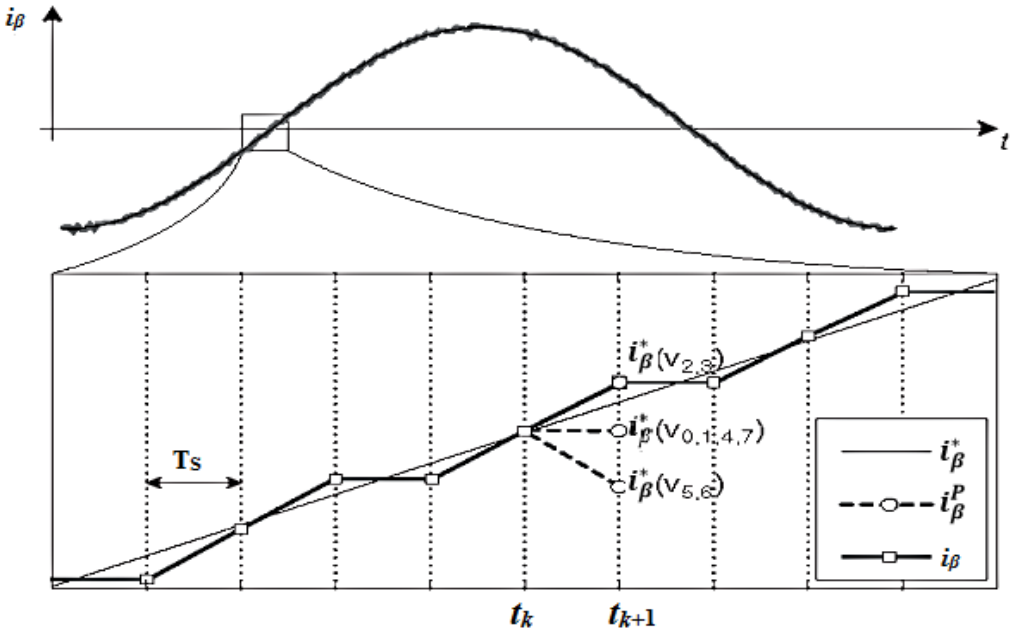


Figure 3.12: Graphical representation of selecting optimal voltage vectors of reference and predicted currents of i_β [73].

3.4 Power Loss Analysis

The power loss occurs due to the switching devices used in the circuit which significantly influences the efficiency of the voltage source inverters. The overall losses in the devices include the conduction, switching and harmonic losses. Collector-emitter voltage and collector-current influence the conduction loss. The reduction of conduction loss requires the decreasing of the collector-emitter voltage during the conduction time, which can only be altered by the manufacturer of the device. Moreover, the temperature of the junction also have an influence on the value of the losses. The mathematical expression for determining the average and instantaneous conduction loss of an IGBT can be expressed as [86], [87].

$$Pcond = \frac{1}{T_0}\int_0^{\frac{T_0}{2}} (V_{ce0} + I_x(t) * R_{ce}) * I_x(t) * \mathcal{T}(t)dt \tag{3.34}$$

$$Pcond_{instantaneous} = (V_{ce0} + I_x(t) * R_{ce}) * I_x(t) * \mathcal{T}(t)dt \tag{3.35}$$

where, V_{ce0} is the turn-on / threshold voltage of the IGBT, R_{ce} is the differential resistance of the IGBT and $I_x(t)$ represents the arm current through the upper IGBT. The value of V_{ce0} and R_{ce} is taken from a manufacturer datasheet at a specified temperature [89]. The mathematical expression of $I_x(t)$ and R_{ce} are as follows.

$$I_x(t) = \left(\frac{I_{dc}}{3}\right) + \left(\frac{I_{ac}}{2}\right) \tag{3.36}$$

$$R_{ce} = \frac{V_{ce2} - V_{ce1}}{I_{ce2} - I_{ce1}} \tag{3.37}$$

The term $\mathcal{T}(t)$ is related with the modulation index m of the controlling method. For PWM only, duty cycle $\mathcal{T}(t)$ is present and its expression can be expressed as [87] -

$$\mathcal{T}(t) = \left(\frac{1}{2}\right) * (1 + m * \sin(2\pi * f_0 * t)) \tag{3.38}$$

Here, the output frequency is indicated by f_0. In case of MPC, there is no need of modulation index. So, in this case this term is neglected.

Moreover, the second loss i.e. the switching loss occurs during the turn-on and turn-off condition of IGBT. The dc link voltages, the output load current, the transient parameters of the IGBTs influence the switching loss. The switching loss is dependent on the junction temperature of the device and the gate driver circuit resistance. This loss can be reduced by using various soft switching techniques. The mathematical expressions for determining the average and instantaneous switching losses are as follows [86], [87].

$$P_{sw} = \left(\frac{1}{T_0}\right) * \int_0^{\frac{T_0}{2}} f_{sw} * \left(E_{on} + E_{off}\right) * \frac{I_x(t)}{I_{ccnom}} * \frac{V_{dc}}{V_{ccnom}} dt \tag{3.39}$$

$$P_{sw\ instantaneous} = f_{sw} * \left(E_{on} + E_{off}\right) * \frac{I_x(t)}{I_{ccnom}} * \frac{V_{dc}}{V_{ccnom}} dt \tag{3.40}$$

where, the switching frequency is presented by f_{sw} , $V_{dc}$is the dc link voltage, V_{ccnom} and I_{ccnom} are the voltage across collector-emitter terminal of IGBT and the collector current during the test, respectively. The values V_{ccnom} and I_{ccnom} are taken from the manufacture datasheet. The values of turn-on and turn-off energy E_{on} and E_{off} , respectively, are also taken from the datasheet [88].

The presence of harmonic the load current also causes power loss. The presence of harmonic component is measured by the term total harmonic distortion (THD). The total harmonic losses due to the harmonic components are determined by the following expression [89].

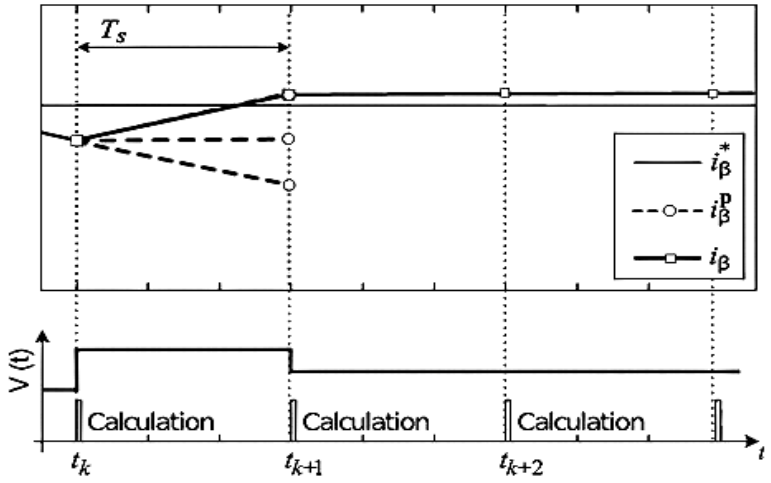
$$P_{harmonic} = 3R_L I_L^2 = 3R_L(I_L^2 + \sum_{n=2}^{\infty} I_n^2) = 3R_L I_1^2(1 + THD_1^2) \tag{3.41}$$

where, I_1, I_n and $THD_1$are the fundamental current, current due to harmonic component and amount of current THD, respectively, and R_L is the per phase load resistance.

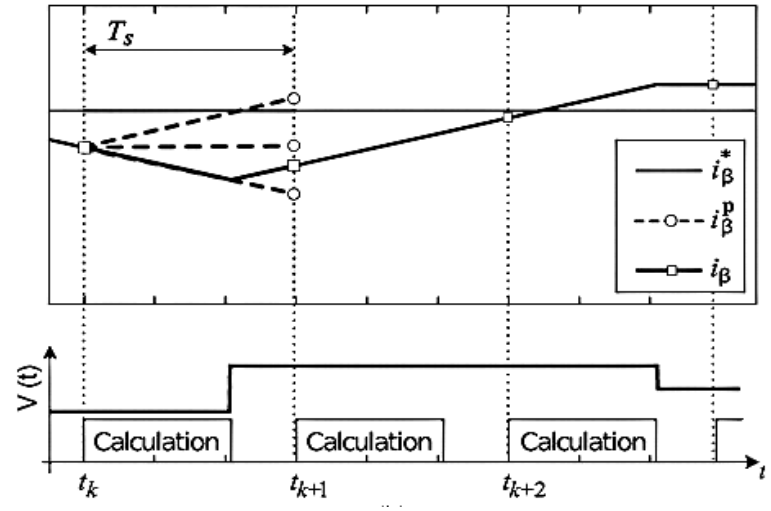
3.5 Delay Compensation

Since the FCS-MPC has many advantages and control parameter flexibility, different control variables as well as different constraints can be included easily in the cost function. However, this type of control scheme requires high amount of calculations in comparison with the classical methods such as PWM. This yields a time delay between the measurements and the application of switching states. The delay between the measurements and the actuation produces ripple in the output current if it is not considered. There is a delay compensation technique available in the literature [90], which is successfully applied to the power converters.

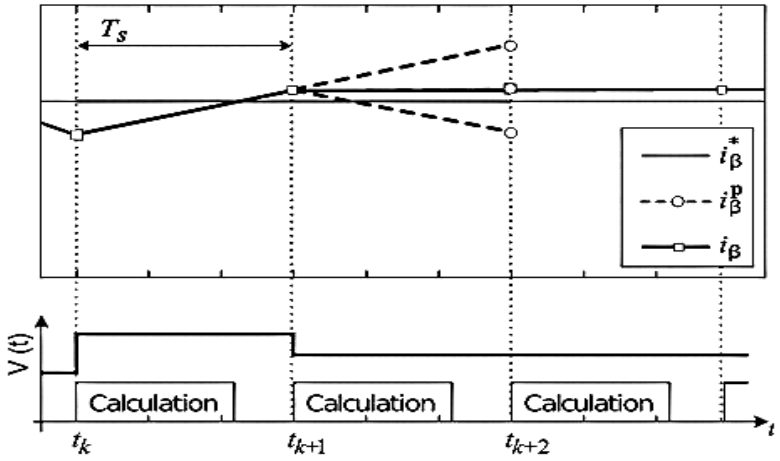
To illustrate the calculation time effect on the current tracking, an ideal case and a real case without and with delay compensation are shown in Figs. 3.13(a), (b) and (c) respectively. Here, only the beta component of the load current (i_β) is shown.



(a)



(b)



(c)

Figure 3.13: Operation of predictive control (a) ideal case: no calculation time required, (b) real case: calculation time is not zero and without delay compensation, (c) real case and with delay compensation [90].

Figure 3.13(a) illustrates the ideal case of the predictive controller i.e. the time required for calculation is zero which is shown here only for comparison. Since the currents are measured at time t_k, instantly the optimal switching state is calculated. The switching state which minimizes the cost function at time t_{k+1} is selected and applied at time t_k. Then, the load current reaches the predicted value at t_{k+1}.

As the SNPC inverter has 32 different voltage vectors, the predicted current in (3.25) and cost function in (3.33) are calculated 32 times. In this case, based on the sampling frequency and the speed of the microprocessor used for the control, the time between the measurement of the load currents and other constraints and the application of the new switching state can be significant.

If the calculation time is significant compared with the sampling time, there will be a delay between the instant in which the currents are measured and the instant of application of the new switching state, as shown in Fig. 3.13 (b). During the interval between these two instants, the previous switching state will continue to be applied. As it can be observed in the figure, the voltage vector selected using measurements at t_k will continue being applied after t_{k+1}, making the load current go away of the reference. The next actuation will be selected considering the measurements in t_{k+1} and will be applied near t_{k+2}. As a consequence of this delay, the load current will oscillate around its reference, increasing the current ripple.

To consider this calculation time period as well as reducing the latency between applied signal and optimum signal, a simple solution is to be taken into account the calculation time as well as apply the selected switching state after the next sampling instant. The proposed control algorithm with delay compensation is shown in the following steps:

Step-1: The load current i(k), capacitor voltages $V_{c1}(k)$ and $V_{c2}(k)$ are measured.
Step-2: Application of the switching state x_{opt} which is calculated in previous interval.
Step-3: Considering the applied switching state, estimate the value of the load currents $i_L(k+1)$ at time t_{k+1}.
Step-4: Prediction of the load currents $i_L^p(k+2)$ for the next sampling instant t_{k+2} for all possible switching states. Also predict the future neutral point voltage $dvc_{12}^p(k+2)$ and evaluate the number of switching transitions n_{sw} for all the possible switching states. Here $i_L^p(k+2)$ is also compared with maximum current limit which is predefined to protect the system from over-current.
Step-5: The designed cost function g_d is evaluated for each of the prediction.
Step-6: For the minimized cost function, g_{opt}, the optimal switching state is selected.

The estimation of $i_L(k+1)$ and the prediction of the load currents are shown in Eqn. 3.42 and Eqn. 3.43 respectively as expressed [73].

$$i_L(k+1) = \left(1 - \frac{\mathrm{RT_s}}{\mathrm{L}}\right) \mathrm{i(k)} + \frac{\mathrm{T_s}}{\mathrm{L}} v(k) \tag{3.42}$$

$$i_L^p(k+2) = \left(1 - \frac{\mathrm{RT_s}}{\mathrm{L}}\right) i_L(\mathrm{k}) + \frac{\mathrm{T_s}}{\mathrm{L}} v(k+1) \tag{3.43}$$

The modified cost function is shown as follows-

$$g_d = \lambda_i\left[i_L^p(k+2) - i_L^*(k+2)\right] + \lambda_{npv}\left[dvc_{12}^p(k+2) - dvc_{12}^*(k+2)\right] + \lambda_{sw}[n_{sw}] + \lambda_{ocp} \quad (3.44)$$

In this research delay compensation algorithm is applied for both the SNPC and NPC topologies.

3.6 Voltage Vector Prediction based MPC

The concept of conventional FCS-MPC is to select an optimal voltage vector which makes the predicted current $i_L^p(k+1)$ close to its reference $i_L^*(k+1)$. Hence, the complex inner loop in MPC is executed for all the possible voltage vectors, which is time consuming. In the voltage vector prediction based MPC [91], the calculations in complex inner loop are simplified by only calculating voltage error rather than the current error. The reference voltage $v^*(k+1)$ is calculated using the measured load current and reference current outside the inner loop. Hence the load current tracks the reference current accurately. Considering the predicted load current in (3.26) and assuming $i_L^*(k+1)$ in place of $i_L^p(k+1)$, the required reference voltage $v^*(k)$ in order to track the reference current can be calculated as [91]-

$$v^*(k+1) = Ri(k) + \frac{L}{T}\left[\, i_L^*(k+1) - i(k)\right] \quad (3.45)$$

Where, $i(k)$ is the measure currents at k sampling time. *R*, *L* and *T* represent resistance, inductance value of per phase load and sampling time for the controller respectively.

This predicted voltage vector is compared to the voltage vectors for 32 different switching states and which minimize the cost function is then selected and applied to the inverter. The cost function will be modified and can be shown in Eqn. 3.46.

$$g_{Vp} = \lambda_v[|v^p(k+1) - v(k)|] + \lambda_{npv}\left[dvc_{12}^p(k+1) - dvc_{12}^*(k+1)\right] + \lambda_{sw}[n_{sw}] + \lambda_{ocp} \quad (3.46)$$

where, $v(k)$ is the voltage vector which is changed for each of the switching state which will be 32 times for SNPC during each sampling time.

Here, $\boldsymbol{v^p}(k+1)$ is considered equal to $\boldsymbol{v}^*(k+1)$ since the sampling frequency of the proposed system is much higher than the system dynamics.

The steps of the algorithm is given below-

Step 1: The load current ***i***(k), capacitor voltages $\mathbf{V_{c1}}$(k) and $\mathbf{V_{c2}}$(k) are measured.
Step 2: Estimation of the reference voltage vector $v^*(k+1)$.
Step 3: For the immediate next sampling instant, the future voltage vector $v^p(k+1)$, the future neutral point voltage $dvc_{12}^p(k+1)$ and evaluate the number of switching transitions n_{sw} are predicted for all the possible switching states.
Step 4: The designed cost function g_{Vp} is evaluated for each of the prediction.
Step 5: For the minimized cost function, g_{opt}, the proper switching state is selected.
Step 6: The newly selected switching state x_{opt} is then applied to the next sampling instant.

This method also known as 'single predictive FCS-MPC' as the optimal voltage vector is selected using a single prediction which reduces the computational time of the controller.

3.7 Selective Voltage Vector based MPC

Further reduction in execution time or runtime can be achieved using selective voltage vector based MPC [91]. In this method, a reduced/selected number of voltage vectors is used instead of using all 32 voltage vectors in each sampling time. The voltage vectors are selected based on the position of the load current in the complex $\alpha\beta$ plane. In order to find the position of the load current. The αβ plane is sub divided into 6 sectors. The location of the load current is determined by-

$$\theta = \tan^{-1}\left(\frac{i_\beta}{i_\alpha}\right) \tag{3.47}$$

where, i_β and i_α are the beta and alpha components of the measured load current.

The sectors of the voltage vectors are shown in the Fig. 3.14.

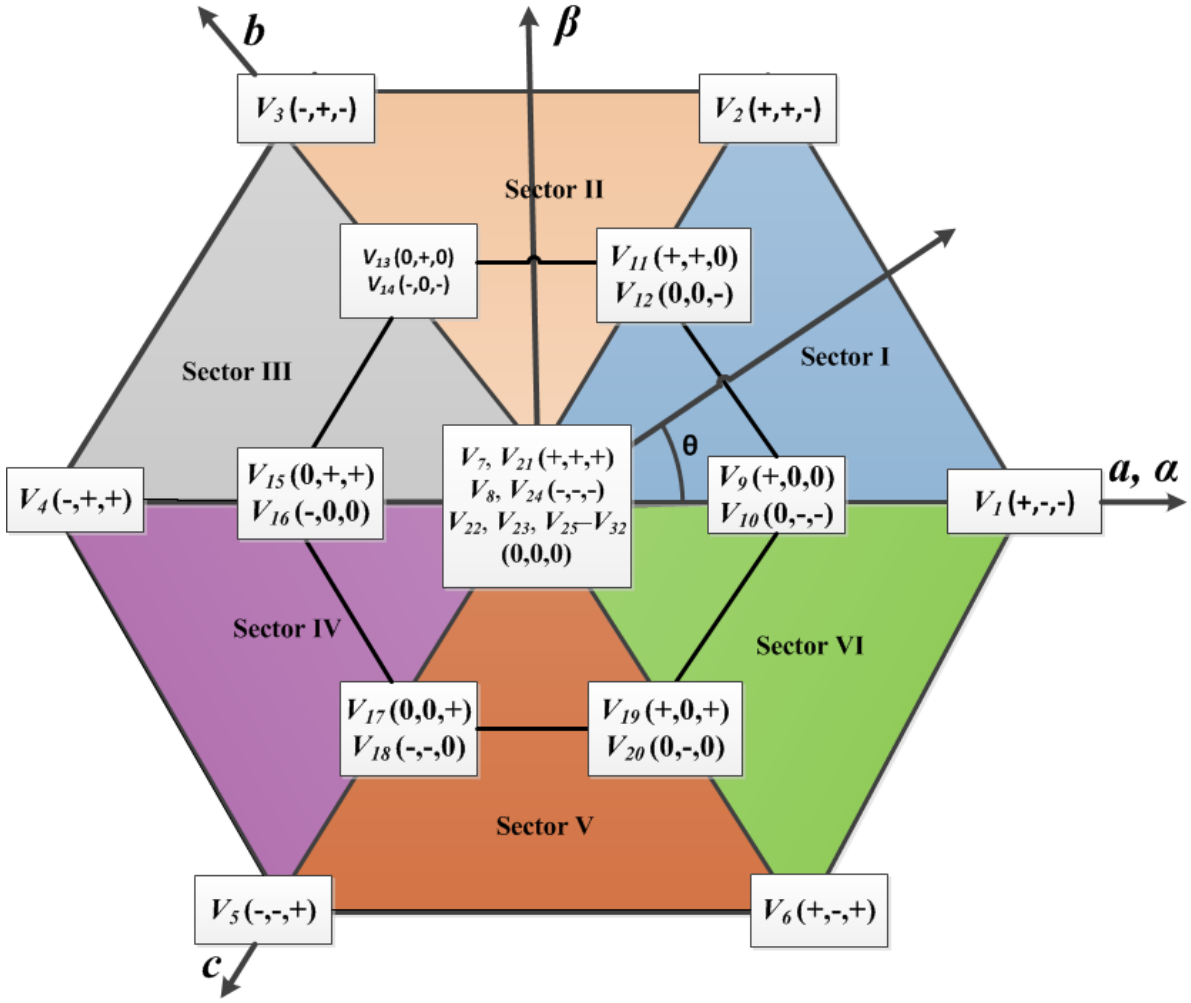


Figure 3.14: Sector distribution in complex $\alpha\beta$ plane.

From Fig. 3.14, it is evident that, the 32 voltage vectors are divided into six sectors. For a particular position of load current, all voltage vectors need not to be evaluated. Only the adjacent voltage vectors are able to track the reference current. During transient, the long vector ahead of upper adjacent or back of lower adjacent may be required to track the reference current.

The voltage vectors taken for the position of load current in each sectors are shown in Table 3.3.

Table 3.3: Voltage vectors for different positions of load current

Sector	Voltage Vectors
I	$\boldsymbol{v_1, v_2, v_3, v_6, v_7, v_8, v_9, v_{10}, v_{11}, v_{12}}$
II	$\boldsymbol{v_1, v_2, v_3, v_4, v_7, v_8, v_{11}, v_{12}, v_{13}, v_{14}}$
III	$\boldsymbol{v_2, v_3, v_4, v_5, v_7, v_8, v_{13}, v_{14}, v_{15}, v_{16}}$
IV	$\boldsymbol{v_3, v_4, v_5, v_6, v_{17}, v_{18}, v_{15}, v_{16}, v_{21}, v_{22}}$
V	$\boldsymbol{v_1, v_4, v_5, v_6, v_{17}, v_{18}, v_{19}, v_{20}, v_{21}, v_{22}}$
VI	$\boldsymbol{v_1, v_2, v_5, v_6, v_9, v_{10}, v_{19}, v_{20}, v_{21}, v_{22}}$

Table 3.3 shows that each sector consists of 10 voltage vectors in which 4 large voltage vectors, 4 small voltage vectors and 2 zero voltage vectors. The selection of zero vectors are done in such a way that the number of switching transition will be minimum. It should be noted that 2 adjacent large voltage vectors ($\boldsymbol{v_3}$ and $\boldsymbol{v_6}$ for sector I) are included in each pool for transient in reference current.

The algorithm of this method is shown in the following steps.

Step-1: The load current $\boldsymbol{i}$(k), capacitor voltages V_{c1}(k) and V_{c2}(k) are measured.
Step-2: Estimation of the reference voltage vector $\boldsymbol{v}^*(k+1)$ and load current position θ.
Step-3: For the immediate next sampling instant, the future voltage vector $\boldsymbol{v^p}(k+1)$, the future neutral point voltage $dvc_{12}^{p}(k+1)$ and evaluate the number of switching transitions n_{sw} are predicted for all the possible switching states.
Step-4: The designed cost function g_{Vp} is evaluated for each of the prediction.
Step-5: For the minimized cost function, g_{opt}, the proper switching state is selected.
Step-6: The newly selected switching state x_{opt} is then applied to the next sampling instant.

Since the number of voltage vectors are reduced from 32 to 10 for each sampling period, the computation burden i.e. execution time is also reduced in great extent.

3.8 Execution Time Calculation Method on dSPACE

The execution time in this research has been performed on dSPACE DS 1104 microprocessor for determining real hardware execution time. This microprocessor can be built using MATLAB/Simulink platform as it has Real time interface (RTI) library which is compatible with MATLAB. The DS 1104 has its own System Control Desk for monitoring the output and

performance of the processor. The method of this calculation is straightforward which is given below:

I. A *Data Store Memory* and *Data Store Read* block from Simulink library have to be added to the model
II. The subsystem whose execution time will be measured should be treated as atomic unit.
III. A *System Outputs Function* block should be added to the atomic subsystem.
IV. The *Data Store Read* should be connected with a *Signal Conversion* block and a terminator.
V. The real time application should be built.
VI. The output signal of the *Data Store Read* block can be observed in the dSPACE System Control Desk plotter

3.9 Summary

In this chapter, the modelling of the inverter load current, neutral point voltage variation, switching frequency, over current protection, and power loss is presented. The mathematical models of different control objectives are then discretized for the controller. The model predictive control strategy is discussed briefly. In order to overcome the time delay between sampling and switching, a delay compensation technique of one step ahead prediction is discussed. Since the proposed MPC for the 3L-SNPC inverter is computationally expensive, two simplified control strategies namely voltage vector prediction based MPC and selective voltage vector based MPC are also dealt in this chapter.

CHAPTER IV

Simulation Results

4.1 Introduction

Multilevel inverter is a power electronic device for power conversion as well as improving power handling capacity. However the multilevel inverters require more number of switching devices which incur high cost and complexity in a control scheme. In this research, a simplified variant of conventional neutral point clamped inverter has been studied. Different model predictive control strategies have been used as a control scheme. To analyze the overall system performance, the current tracking accuracy, neutral point voltage balancing, voltage stress on the switching devices, switching frequency, common mode voltage, and power loss in the switching devices are presented. A comparative study between NPC and SNPC are also presented in this chapter.

4.2 Performance Analysis of the Proposed SNPC

A 6 KVA SNPC inverter has been designed for delivering 8A current to three phase RL load with 415V line to line output voltage. The whole simulations are carried out by using MATLAB/Simulink tool. The model designed in the MATLAB/Simulink platform is shown in Fig. 4.1. During simulation, 587V dc link voltage is maintained constant and the sampling time of 25μs is considered. The solver taken during this simulation is ode5 (Dormand-Prince) with fixed step size of 25μs. The parameters required by the blocks of the model are initialized in a separate m-file and it needs to be executed every-time before starting the simulation. The parameters utilized in the simulation are shown in Table 4.1.

Table 4.1: Parameters for the simulated systems.

Parameter	Value
Dc link voltage	587V
Reference current	8A
Reference frequency	50Hz
Load resistance	25Ω
Load inductance	10mH
Capacitor	3900μF
Sampling time	25μs

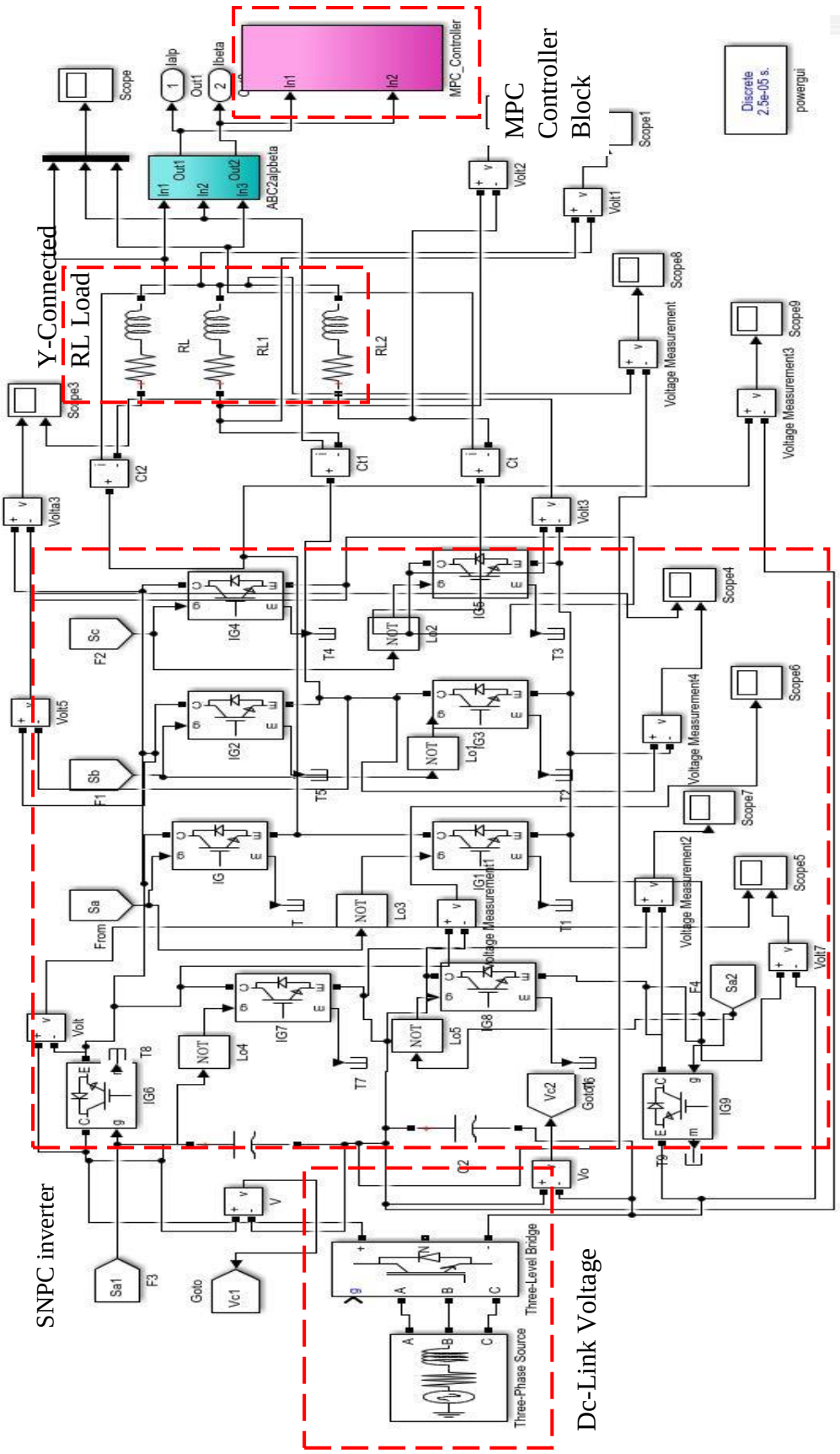


Figure 4.1: MATLAB/SIMULINK representation of the proposed MPC based SNPC inverter.

4.2.1 Switching frequency reduction and its impact

The switching frequency is directly related to the switching loss of the inverter. In order to reduce the switching frequency, a switching transition term is included in the cost function with a weighting factor λ_{sw}. The switching frequency, current THD and neutral point voltage with the variation of λ_{sw} are represented in Table 4.2.

Table 4.2: Current THD, neutral point voltage and switching frequency variation with λ_{sw}.

Weighting factor, λ_{sw}	Current THD [%]	Switching frequency [KHz]	Peak neutral point voltage [V]
0	2.33	8.96	0.058
0.002	2.33	8.17	0.06
0.009	2.36	5.01	0.09
0.01	2.39	4.94	0.09
0.02	2.52	4.11	0.19
0.03	2.55	2.66	2.20
0.04	2.57	2.54	2.20
0.06	2.68	2.39	2.30
0.07	2.80	2.27	2.43
0.1	3.00	1.98	2.55

An optimal λ_{sw} is selected by considering the variation of both current THD and switching frequency and a trade-off is made between them as shown in Fig. 4.2. In Fig. 4.2, it is shown that the optimum value of λ_{sw} is 0.0123. It should be mentioned here that, the weighting factor λ_{npv} is set as 0.4 throughout the analysis.

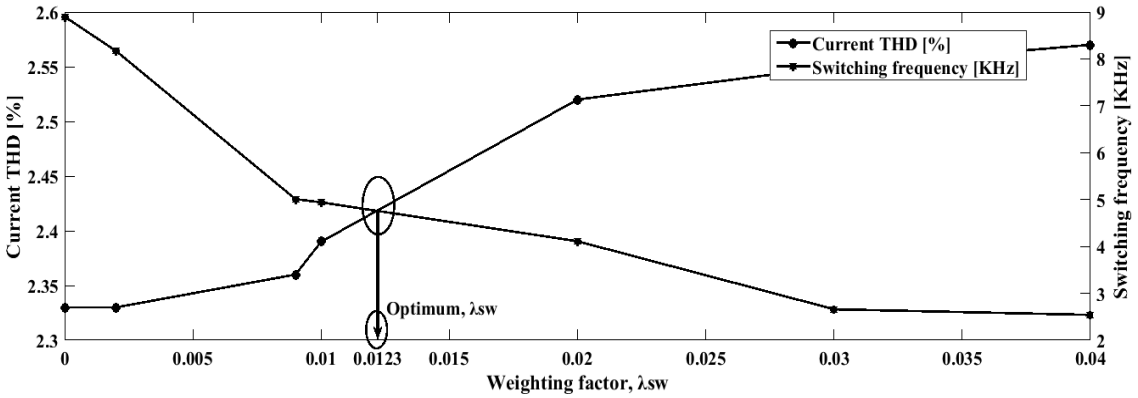


Figure 4.2: Selection of optimum weighting factor, λ_{sw} for the proposed control strategy.

4.2.2 Steady-state current analysis

The performance of the proposed SNPC is analyzed through the steady-state response of the system. A sinusoidal reference current of 8 A and 50 Hz is used. In Fig. 4.3, the steady state response of the three phase load current without delay compensation is shown. It can be seen that the load currents follow the reference phase currents with small deviation. An improved steady state current response is achieved by implementing delay compensation and is shown in

Fig. 4.4. It can be seen that the load currents track the reference current accurately. Due to this delay compensation, the current THD is improved from 2.33% to 2.27%, and the switching frequency is improved from 4.9 KHz to 4.51 KHz as can be seen in the next sub-section 4.2.3.

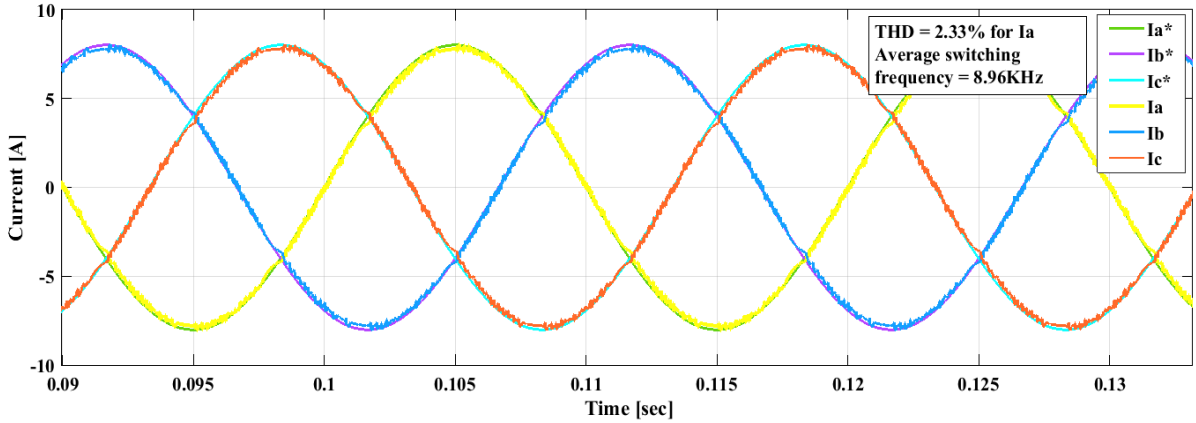


Figure 4.3: Steady state three phase load current of the proposed SNPC inverter without delay compensation.

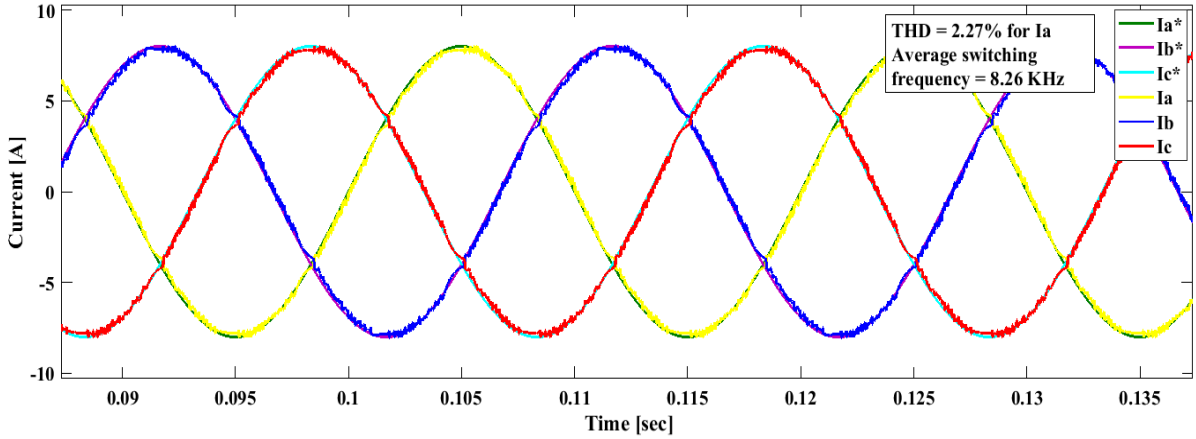


Figure 4.4: Steady state three phase load current of the proposed SNPC inverter with delay compensation.

4.2.3 Current THD analysis

To calculate the THD for I_a, FFT is performed and 2.27% current THD has been found with considering delay compensation which is shown in Fig. 4.5. The FFT is also performed without considering delay compensation and shown in Fig. 4.6. Moreover, the controller with delay compensation yields the average switching frequencies of 8.26 KHz and 4.51 KHz while the controller without delay compensation yields 8.96 KHz and 4.9 KHz when the switching frequency term is excluded and included in the cost function respectively.

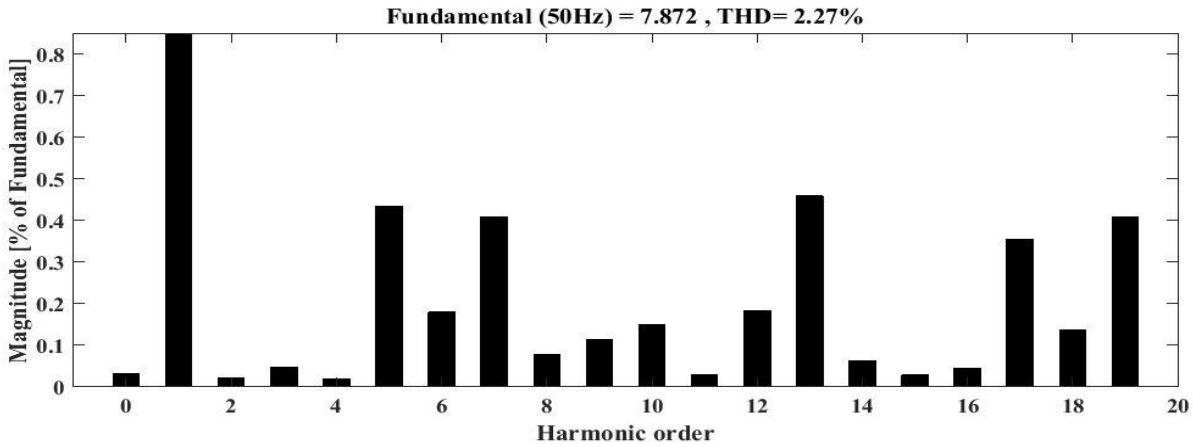


Figure 4.5: Current THD of phase ‘a’ with delay compensation.

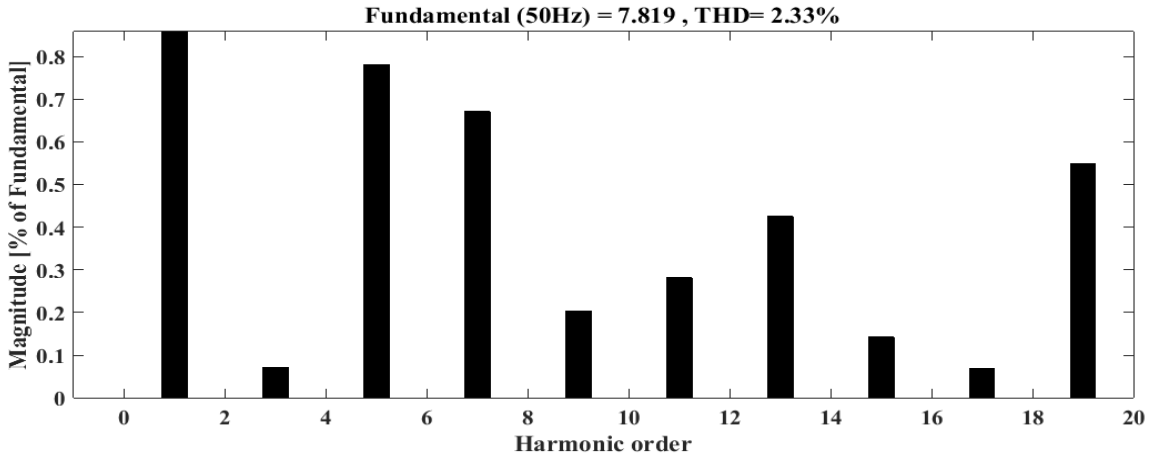


Figure 4.6: Current THD of phase ‘a’ without delay compensation.

Form Figs. 4.5 and 4.6, it is seen that the current THD is increased by .06% while the switching frequency reduced by 4.45 KHz (49.66%).

4.2.4 Steady state voltage analysis

The voltage between ‘a’ phase and neutral point of the inverter (V_{aN}) is shown in Fig. 4.7 for illustrating that three voltage levels ($\pm\frac{V_{dc}}{2}, 0$) are achieved from the multilevel inverter system.

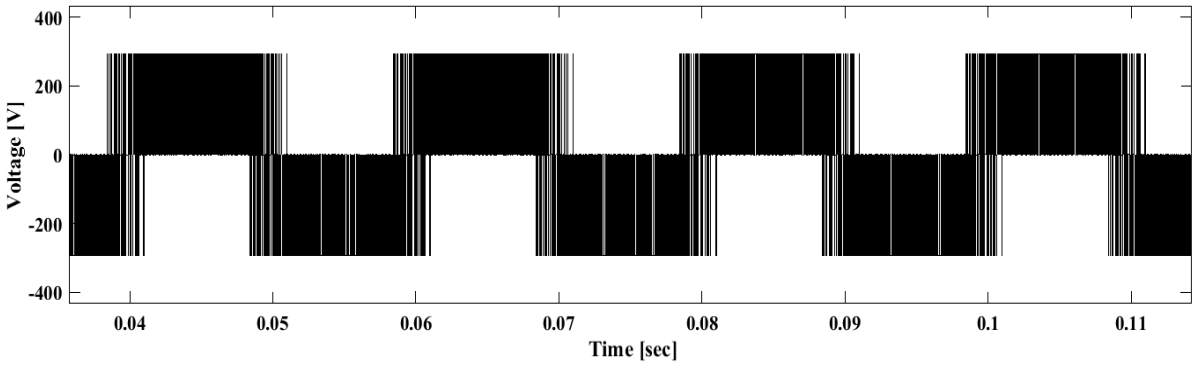


Figure 4.7: Steady state voltage between ‘a’ phase and neutral point of the inverter.

Steady state line to line (V_{ab}, V_{bc}, V_{ca}) for three phases are shown in Fig. 4.8. By observing Fig. 4.8, 120^0 phase shift among the line voltages are realized.

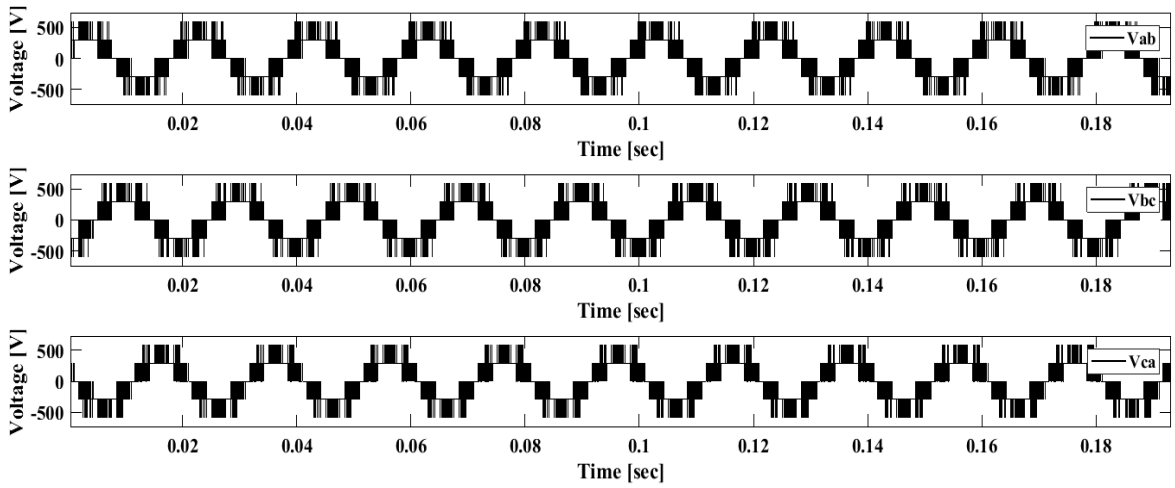


Figure 4.8: Zoomed steady state line to line voltage (V_{ab}, V_{bc}, V_{ca}) at the SNPC inverter output.

4.2.5 Transient response analysis

To evaluate the performance of the proposed controller at transient condition, a step down command in reference current I_α^* is applied at 0.34sec. The current waveforms for transient reference tracking is shown in Fig. 4.9. It can be seen that the controller tracks the reference current expeditiously at transient without any overshoot/undershoot. Moreover, the change in alpha component has no effect on the beta component which ensures decoupled control. This decoupled control feature yields fast transient response.

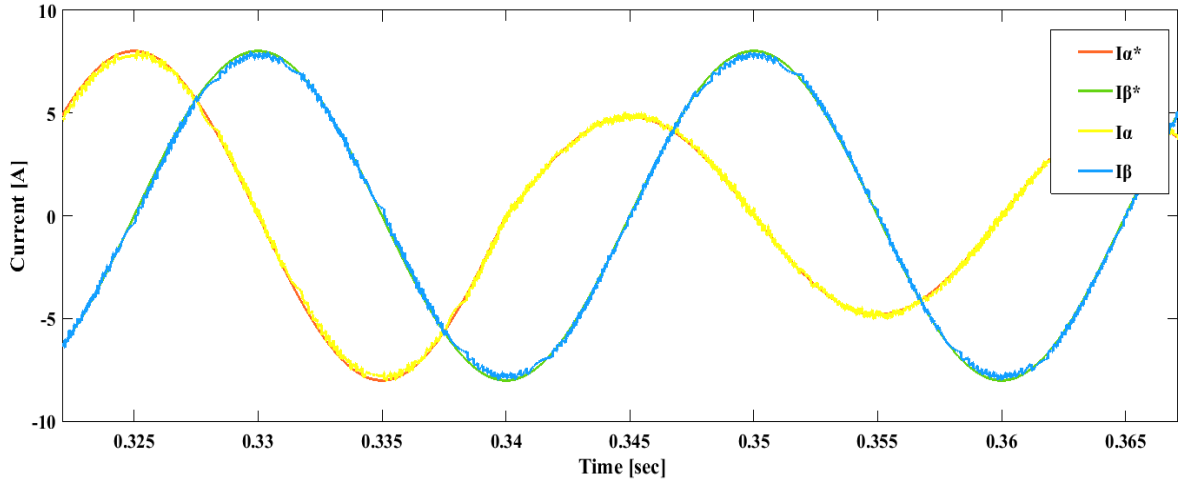


Figure 4.9: Current tracking accuracy during step down command and decoupling control of the proposed system.

The transient response of the proposed controller is further tested for a step up command in reference current I_α^* and shown in Fig. 4.10. Initially I_α^* is set to zero, then at 0.205sec the maximum value of I_α^* is set to 8 A. It can be seen that the load current reaches the reference current quickly; the response time is 0.3ms which is clear from Fig. 4.11. Note that another

current component (I_β) is completely unaffected. The effect of the step up current command on the three phase currents is also illustrated in Fig.4.12.

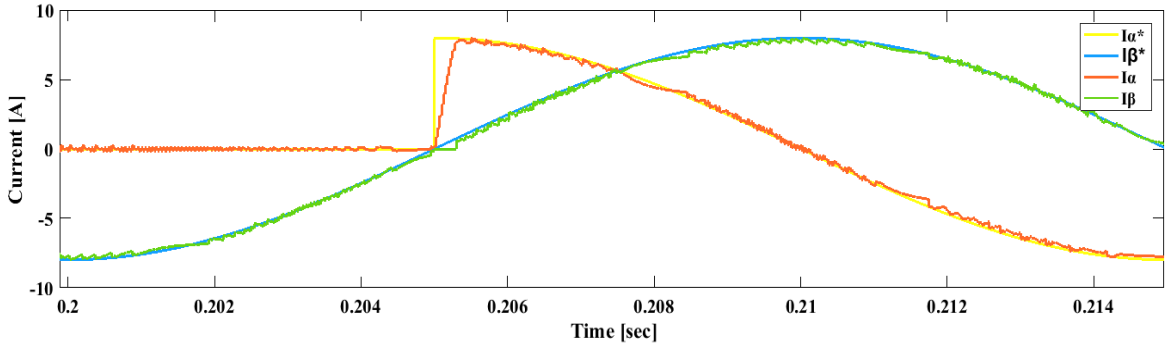


Figure 4.10: Transient response of the proposed control strategy during step up current command.

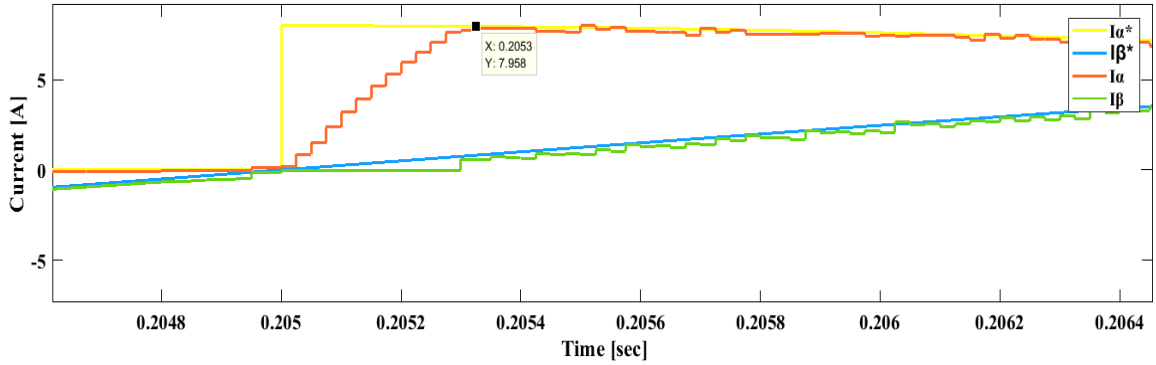


Figure 4.11: Zoomed transient response of the proposed control strategy during step up current command.

From the Fig. 4.11, the response time can be calculated easily which is 0.0003 sec or 0.3ms. The effect on the three phase current is illustrated in Fig.4.12.

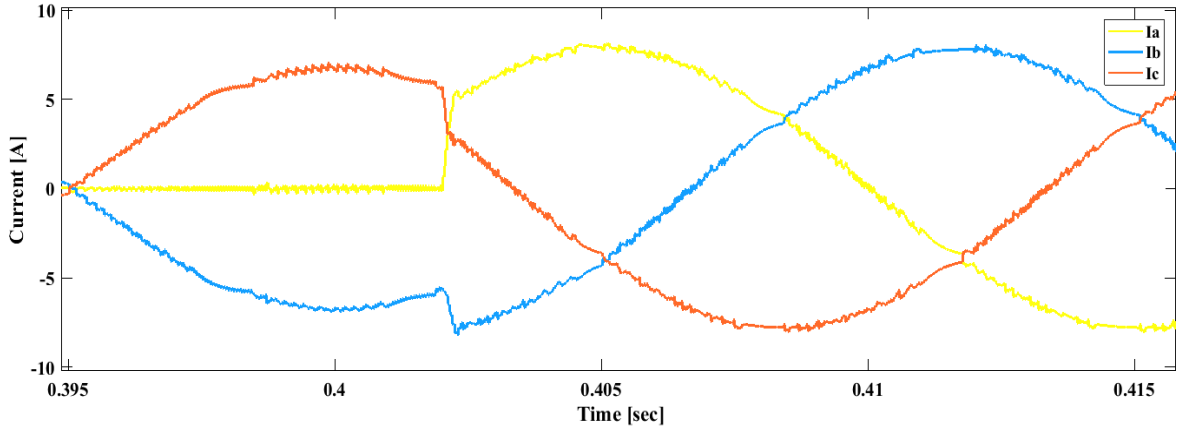


Figure 4.12: Three phase transient current responses during step up current command.

4.2.6 Neutral point voltage balancing

A neutral point clamped inverter topology has a great concern to balance the neutral point voltage. It is because neutral point voltage introduces ripple in the output currents. The neutral

point voltage variation for the propose system is shown in Fig. 4.13. It can be seen that the voltage variation at the neutral point is close to zero. This means that two capacitor voltages are balanced properly. The peak voltage variation is 0.06V which is within an acceptable range.

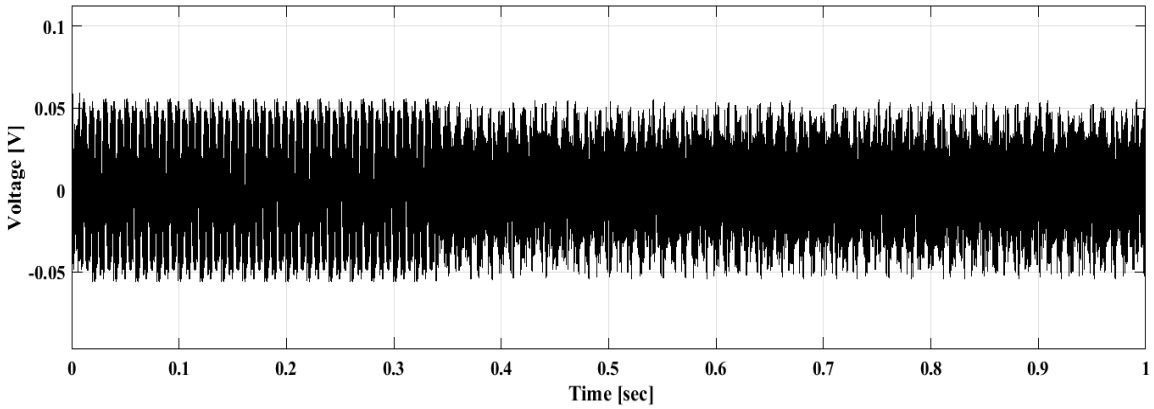


Figure 4.13: Neutral point voltage balancing of the proposed system.

To verify the controller for capacitors voltage balancing, the weighting factor λ_{npv} in the cost function is changed to 0 from 0.4 at t=0.3 sec. If $\lambda_{npv} = 0$, the cost function does not consider the neutral point voltage, which affects the voltage balancing as shown in Fig. 4.14. It is seen that two capacitor voltages are perfectly balanced before 0.3sec. Once λ_{npv} set to 0, two capacitor voltages become unbalanced. Hence, the controller takes care of neutral point voltage variation in a very intuitive way by considering it as an objective in the cost function.

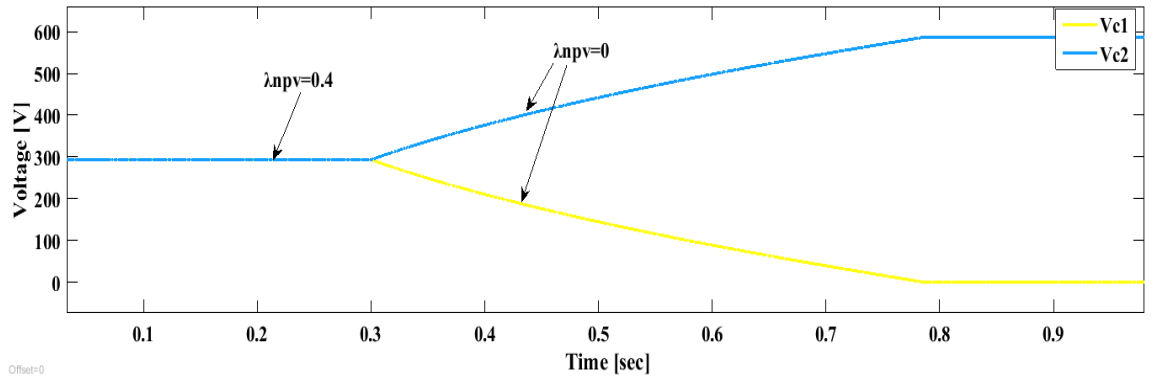


Figure 4.14: Verification of the controller's neutral point voltage balancing ability.

4.2.7 Voltage stress analysis

To analyze voltage stress across semiconductor switches, voltage is measured across different switches and the voltage waveforms across S_1, S_2, S_3, and S_4 (3 level dc side) is shown in Fig. 4.15. It is observed that the voltage stress on each switch is maximum $\frac{V_{dc}}{2}$ volt. However, the stress across the switch in each arm of 2 level inverter is V_{dc}volt as can be seen in Fig. 4.16.

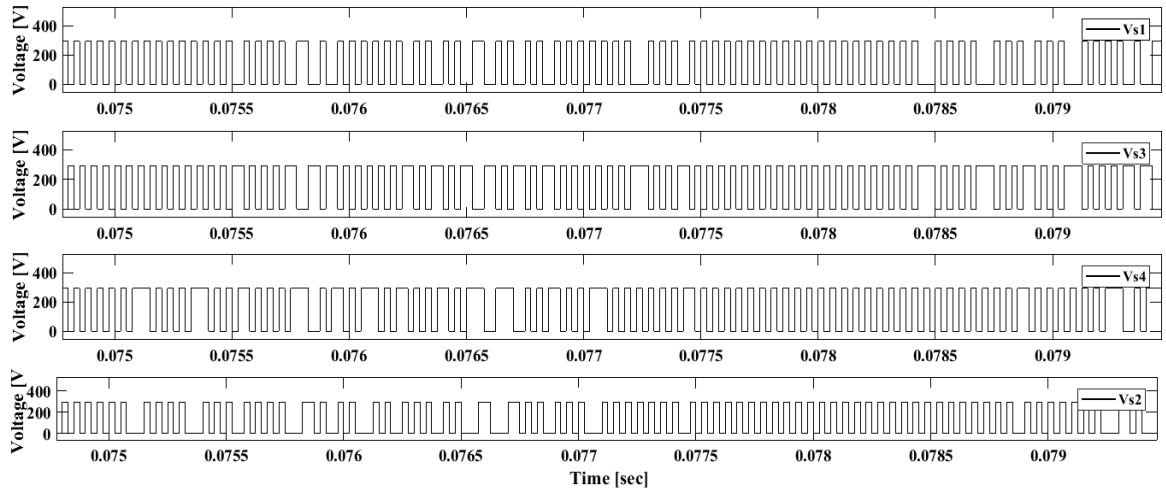


Figure 4.15: Voltage stress across four switches of 3-level dc side of the SNPC inverter.

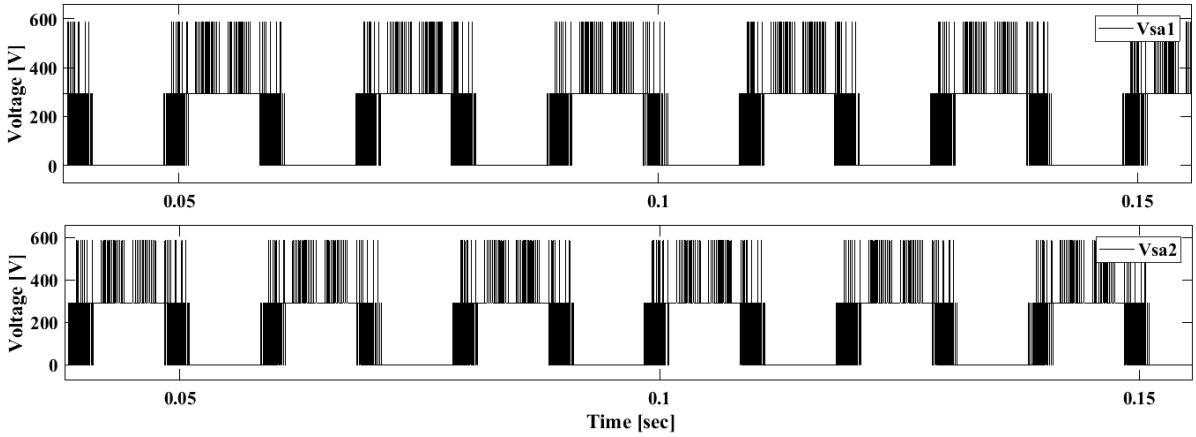


Figure 4.16: Voltage across two switches located at ‘a’ phase arm of the 2 level inverter side of SNPC inverter.

4.2.8 Common mode voltage analysis

Common mode voltage reduction is an important factor while deploying on-grid application and also for motor driver application. To determine the common mode voltage a voltage across the neutral of the Y-connected three phase load and the neutral point of the capacitor is measured and shown in Fig. 4.17. From Fig. 4.17, it is clearly seen that the common mode voltage is in the range of $\pm\frac{V_{dc}}{3}$ volt.

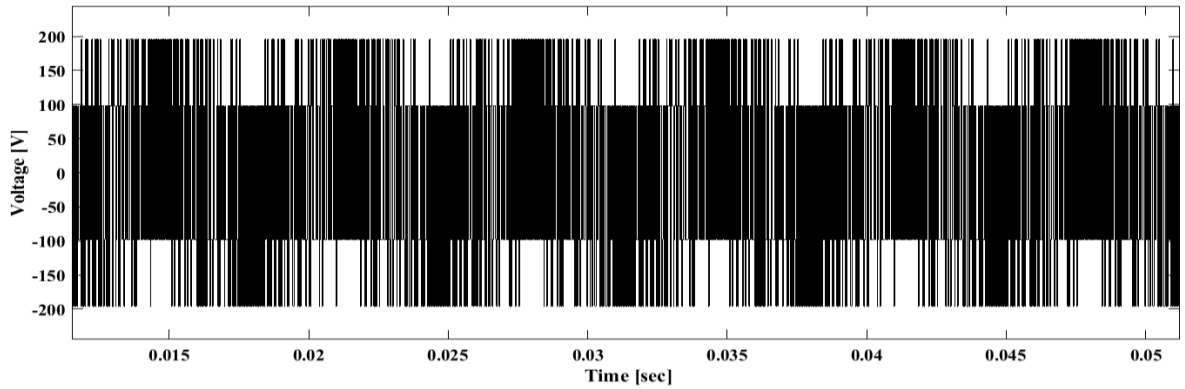


Figure 4.17: Common mode voltage of the proposed inverter system.

4.2.9 Over-current protection

The proposed MPC based SNPC inverter system is protected from over current. In Fig. 4.18, the over current protection of the proposed system and its effectiveness is shown. By observing Fig. 4.18, it is realized that the current is not exceed its maximum rating 15A though the reference current peak is taken as 20A for evaluating the protection scheme.

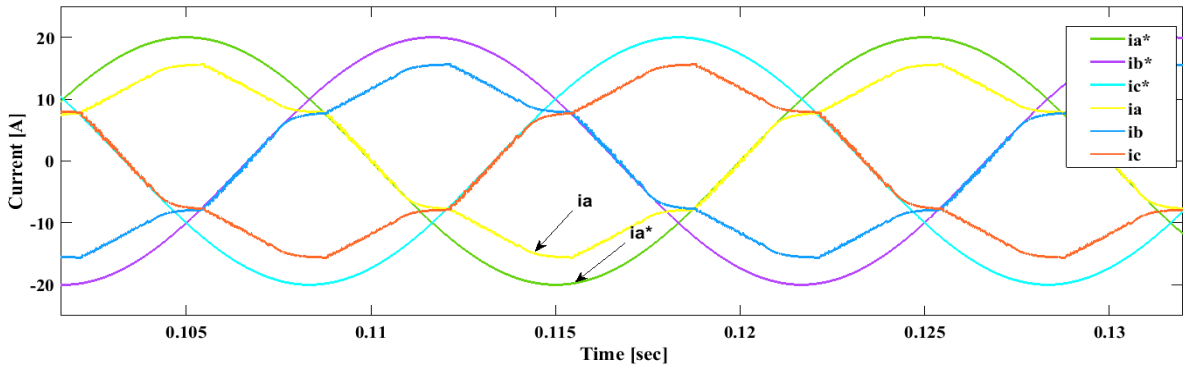


Figure 4.18: Three phase current waveforms (i_a, i_b, i_c) along with the reference current (i_a^*, i_b^*, i_c^*).

4.2.10 Power loss analysis

To verify the proposed controller performance, different type power losses are analyzed in this sub-section. The parameters used in the analysis are shown in Table 4.3 and the related expressions have already been presented in the preceding chapter.

Table 4.3: Parameters used for the power loss analysis.

Parameters	**Value**	**Parameters**	**Value**
Switching frequency, fsw	4.9 kHz	DC link voltage, V_{dc}	587 V
Turn-On energy, E_{on}	1.4 mJ	Turn-on/Threshold voltage of IGBT, V_{ce0}	1.5 V
Turn-off Energy, E_{off}	2.0 mJ	Output frequency, f_o	50 Hz
Voltage across V_{ce} during Test, V_{ccnom}	587 V	Weighting factor, λ_{npv}	0.4
Collector Current during Test, I_{cnom}	8 A	IGBT differential resistance, R_{ce}	25Ω

Three different losses are considered: switching loss, conduction loss and harmonic loss. The effect of weighting factor, λ_{sw} upon switching loss and conduction loss is shown in Table 4.4.

Table 4.4: Variation of switching and conduction losses with weighting factor, λ_{sw}

Weighting factor, λ_{sw}	Switching loss [W]	Conduction loss [W]
0	2.8684	5.7179
0.001	2.7127	5.7180
0.002	2.7127	5.7180
0.009	1.6030	5.7183
0.01	1.5785	5.7124
0.0123	1.5677	5.7117
0.02	1.3235	5.7231
0.03	0.8516	5.7264
0.04	0.7663	5.7316
0.06	0.7297	5.7323
0.07	0.7297	5.7500

To visualize the pattern of the variation the graphical representation is given in Fig. 4.19.

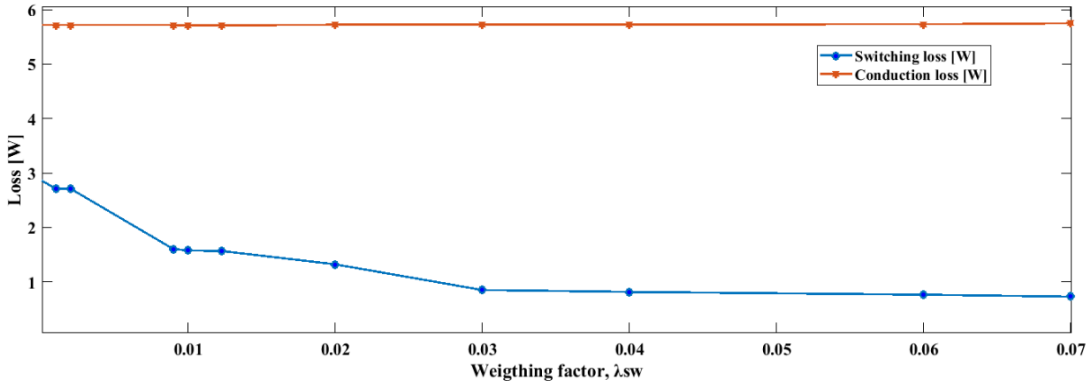


Figure 4.19: Variation of switching and conduction losses with weighting factor λ_{sw}.

From the above illustration, it is clearly seen that the switching loss is reduced with the increase of λ_{sw}. This can be understood by the fact that, as the switching frequency reduces, the corresponding switching loss can also be reduced. At the optimum point of λ_{sw}, the switching loss is 1.5677W and without the switching transition term it becomes 2.8684W. So, a high percentage such as 45.34% loss can be depleted by this optimization strategy. The conduction loss is not changed that much over the variation of the weighting factor, λ_{sw} since it is not direct function of switching frequency. However a slight variation is evident in the conduction loss as the cost function carries other constraints which has indirect effect of the rising of λ_{sw}. Harmonic loss is also calculated for both without and with switching frequency transition term. The data is shown in Table 4.5.

Table 4.5: Effect of switching frequency term on harmonic loss

Weighting factor, λ_{sw}	Harmonic loss [W]
0	0.0804
0.0123	0.124

From the Table 4.5, it is evident that the harmonic loss is increased as the weighting factor, λ_{sw} is increased. Since switching frequency is reduced with the increase of λ_{sw}, the THD is increased so the harmonic loss also increased. The effect of operating at the optimum point is described in tabular form in Table 4.6 below.

Table 4.6: Effect of optimum point on power loss

Weighting factor, λ_{sw}	Switching loss [W]	Conduction loss [W]	Harmonic loss [W]	Total loss [W]
0	2.8684	5.7179	0.0804	8.667
0.0123	1.5677	5.7117	0.124	7.4037

4.3 Comparative Analysis with the Conventional 3-level NPC Inverter

The proposed 3-level inverter is actually one of the simplified variants of the conventional neutral point clamped (NPC) or diode clamped inverter. To evaluate the proposed inverter's performance and quality, a comparative study is required. To do so, a conventional diode clamped 3-level NPC inverter is considered. The same finite state predictive current control is used for conventional NPC with similar operating condition to SNPC. The optimum operating point is determined in a similar fashion and is shown in Fig. 4.20.

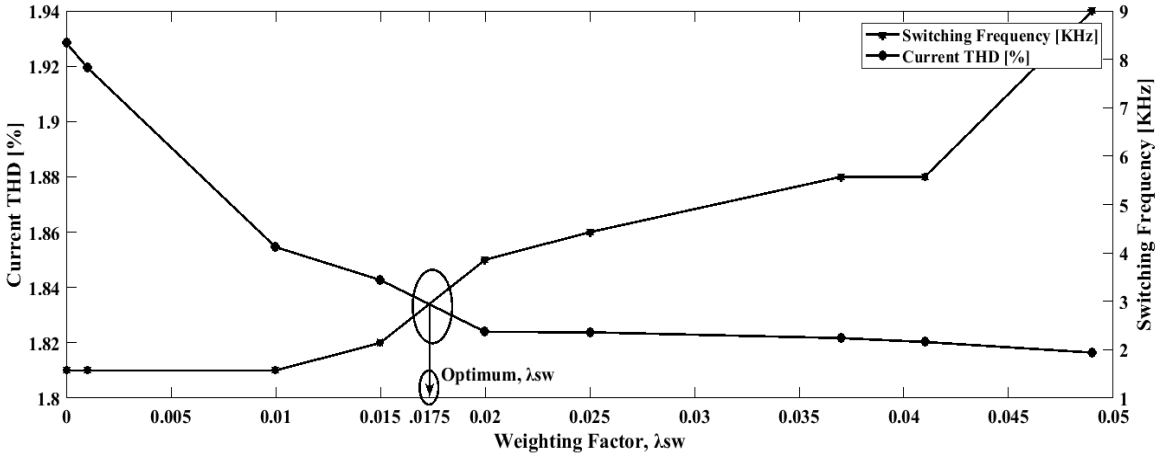


Figure 4.20: Optimum operating point selection for conventional 3L-NPC.

4.3.1 Comparison in terms current THD and switching frequency reduction

At the optimum point of operation the current THD for NPC is analyzed and shown in Fig. 4.21.

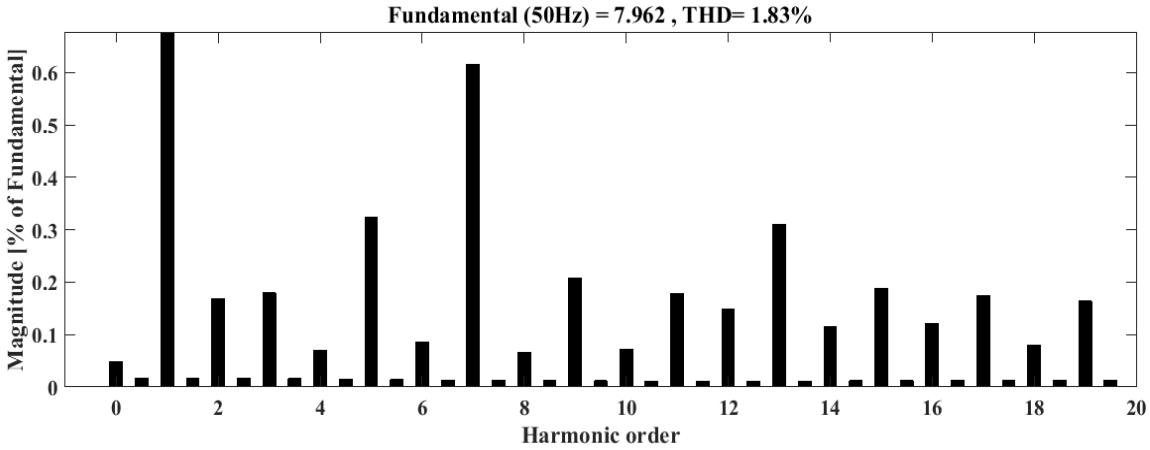


Figure 4.21: Current THD for 3L-NPC at the optimal operating point.

From the above illustration, it is evident that 1.83% current THD is incurred at the optimum point with switching frequency of 2.46 KHz. The proposed system offers 2.31% current THD with 4.51 KHz switching frequency. Without considering switching transition term (STT) in the cost function, 2.27% and 1.81% current THDs having average switching frequency of 8.96 KHz and 8.34 KHz are found for SNPC and NPC, respectively. The comparisons are shown Fig. 4.22 and Fig. 4.23 in a bar chart.

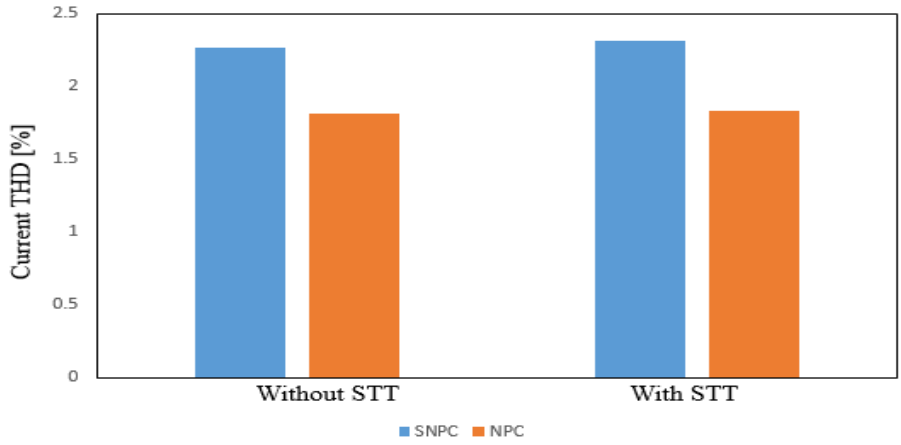


Figure 4.22: Comparison of SNPC and NPC with respect to current THD.

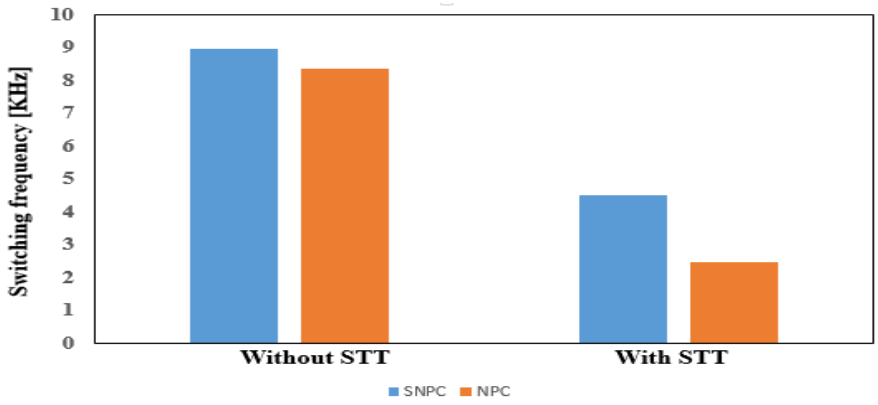


Figure 4.23: Comparison between SNPC and NPC with respect to switching frequency reduction.

The percentage reduction in switching frequency for SNPC is 49.66% whereas for NPC it is 70.5% which is superior to SNPC. Moreover, the NPC inverter sacrifices 0.02% of current THD whereas SNPC sacrifices 0.04%.

4.3.2 Comparison in terms of capacitor voltage balancing

The capacitor voltage balancing constraint is included in the cost function with weighting factor, λ_{npv}=0.4 for both SNPC and NPC configurations and kept constant throughout the simulation. Since the term λ_{sw} is tuning for achieving optimal point, the effect of capacitor voltage balancing is important to check. The variation of capacitor voltage balancing with respect to λ_{sw}tuning is shown in Table 4.7 for both the SNPC and NPC configurations.

Table 4.7: Variation of neutral point voltage with respect to weighting factor, λ_{sw}

Weighting factor, λ_{sw}	For SNPC	For NPC
	Maximum neutral point voltage (V)	Maximum neutral point voltage (V)
0	0.058	0.065
0.001	0.06	0.065
0.02	0.19	1.5
0.04	2.2	1.55
0.05	2.3	5.2

From Table 4.7, it is obvious that the SNPC performs better than NPC as it shows less voltage imbalance with respect to NPC. As SNPC does not have medium voltage vectors, which connect the three-phase output to the 3 different levels of dc link simultaneously resulting charging and discharging of capacitor voltages depending on regeneration and loading condition respectively.

4.3.3 Comparison in terms of transient response analysis

The transient response of NPC is performed in the similar way to the transient analysis of SNPC. The transient response and response time is calculated and shown in Fig. 4.24 and Fig. 4.25, respectively.

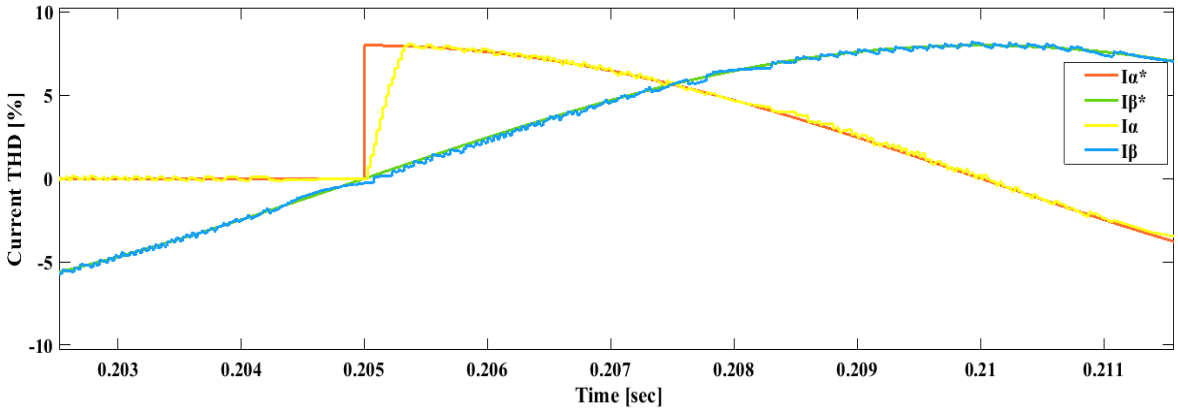


Figure 4.24: Transient response analysis of 3L-NPC.

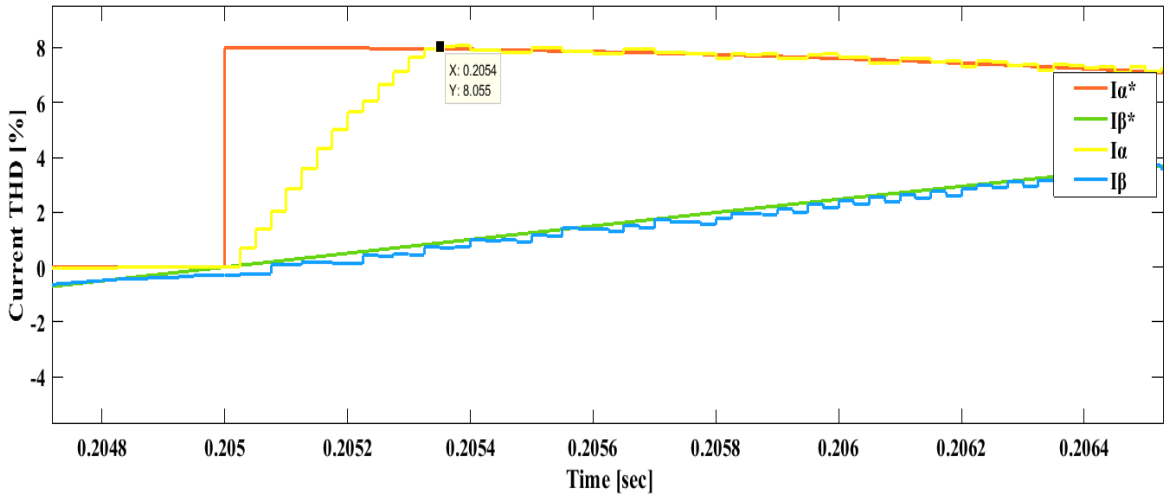


Figure 4.25: Zoomed transient response analysis of 3L-NPC.

From the above illustration, the load current tracks the reference current within 0.4 ms which is similar to the SNPC.

4.3.4: Comparison in terms of power loss analysis

The procedure which is followed for SNPC is also applied to NPC for power loss analysis. The Comparative analysis of switching loss, conduction loss and harmonic loss between SNPC and NPC is shown in Table 4.8. From Table 4.8, it is obvious that the NPC inverter yields lower loss than the SNPC. This is because more number of switching happens in the proposed SNPC inverter. The dc link capacitors charge and discharge through switching. The total loss incurred by the SNPC is 7.403W whereas total loss for NPC is 5.0589 W. The total loss is 46.34% higher in SNPC with respect NPC.

Table 4.8: Comparative power loss analysis between SNPC and NPC

Type of loss	Loss for SNPC (W)	Loss for NPC (W)
Switching loss	1.5677	0.4309
Conduction loss	5.7117	4.5763
Harmonic loss	0.124	0.0517
Total loss	7.4034	5.0589

The bar chart representation for the comparative analysis of power losses is illustrated in Fig. 4.26.

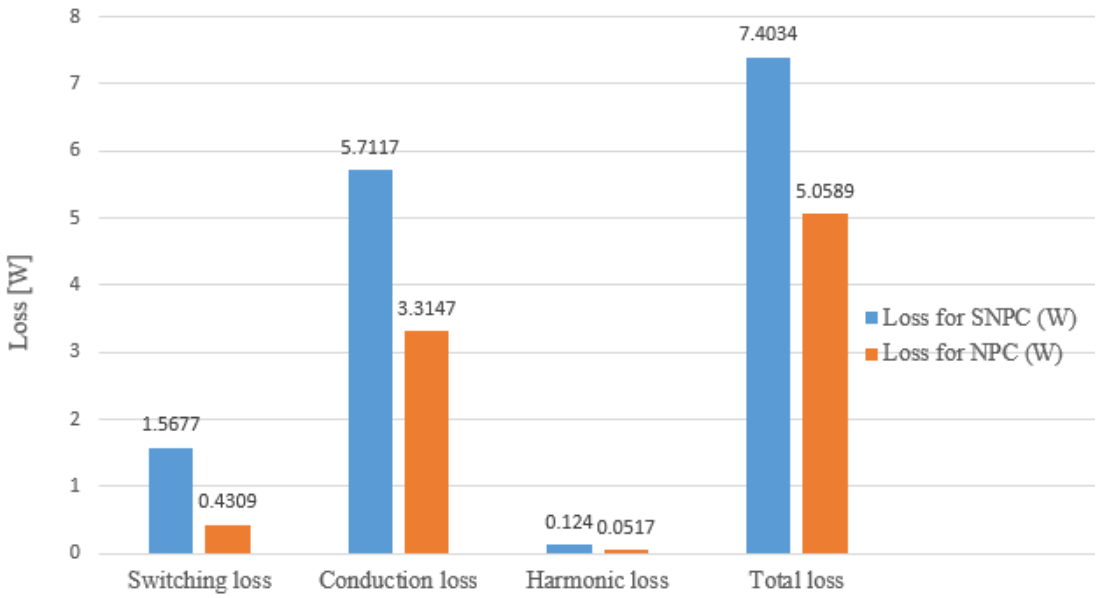


Figure 4.26: Power loss analysis of SNPC and conventional NPC.

It is obvious from the comparative analysis between SNPC and NPC that the NPC is superior in most of the aspects. However, SNPC is superior in terms of neutral point voltage balancing. Moreover, it requires less amount of switching components and thus designing control scheme is less complex. This enhances the system reliability.

4.4 Voltage Vector Prediction based MPC

In the proposed system, the model predictive current control is further simplified by using the voltage vector prediction. Here, the steady state three phase load current responses are shown in Fig. 4.27.

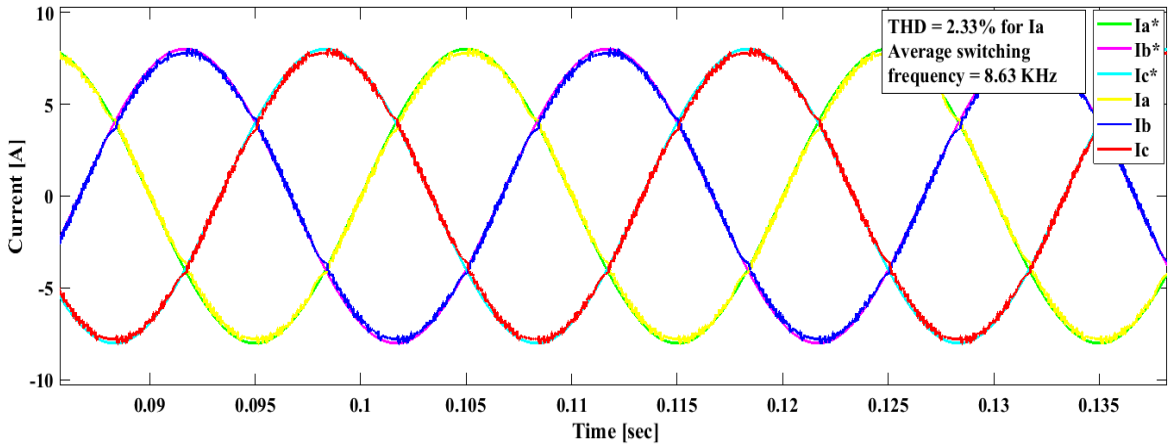


Figure 4.27: Steady state three phase load current responses for the voltage vector prediction based MPC.

To calculate the current THD in the output load current FFT analysis is performed. The current THD of ‘a’ phase is shown in Fig. 4.28. It should be mentioned here that the current THD is calculated without using switching frequency term in the cost function.

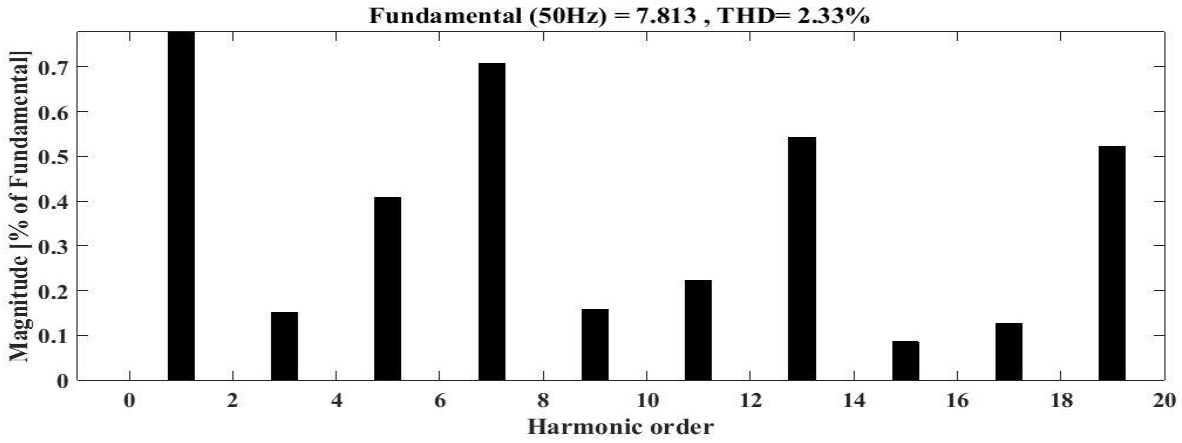


Figure 4.28: FFT analysis of phase 'a' current for the voltage vector prediction based MPC.

From the Fig. 4.28, it is clearly realized that the current THD is similar to delay compensated FCS-MPC which is used in our proposed system. However this voltage vector prediction based MPC offers lower execution time that is important for hardware implementation.

The transient response for the voltage vector prediction based MPC is also demonstrated using step change in the alpha component of the reference current. The transient response is also determined by using data cursor. The zoomed illustration of the transient response is shown in Fig. 4.29.

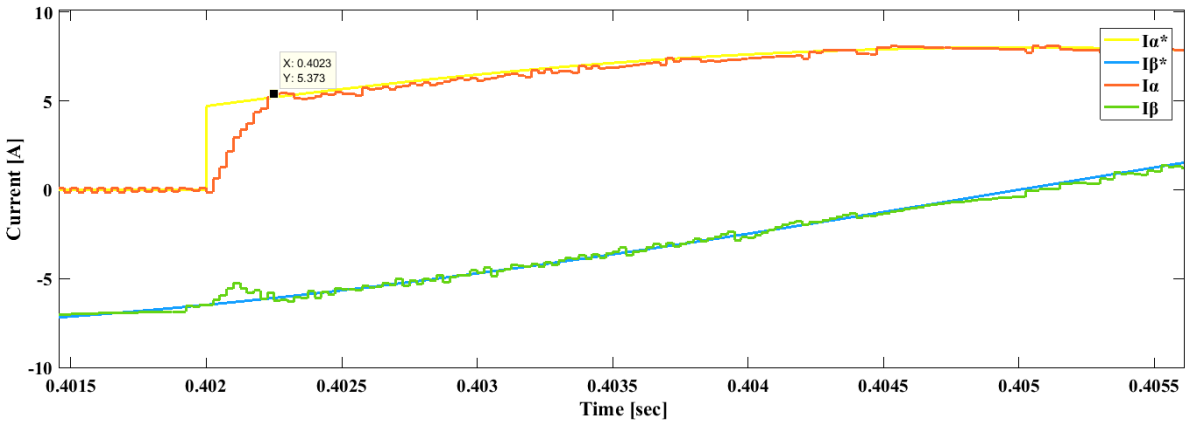


Figure 4.29: Zoomed current transient response analysis for the voltage vector prediction based MPC.

From Fig. 4.29, it can be seen that the load current settle time is nearly 0.3 ms which is identical with the proposed system.

4.5 Selective Voltage Vector based MPC

The steady state current response of selective voltage vector based MPC is shown in Fig. 4.30.

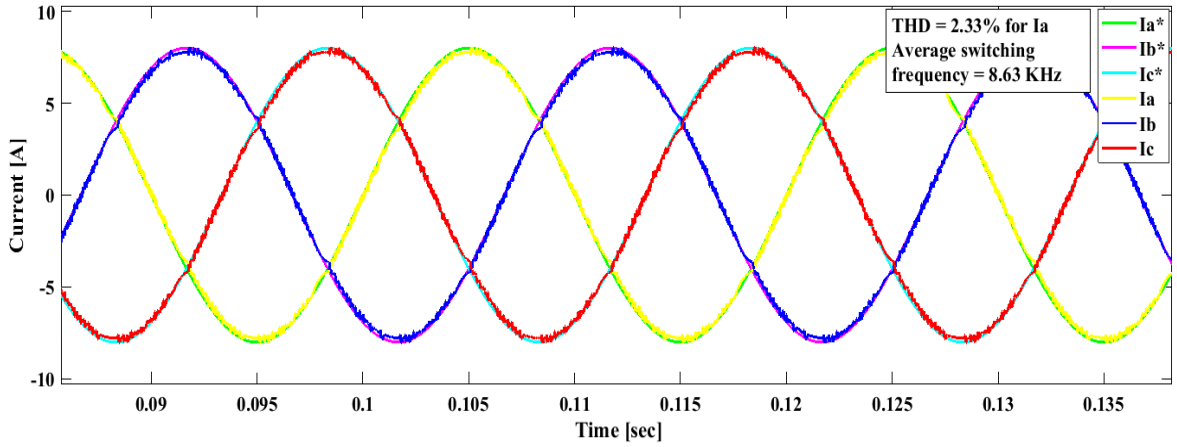


Figure 4.30: Steady state three phase load current responses for the selective voltage vector based MPC.

Fig. 4.30 illustrates that the current response is in acceptable limit. For clear idea, FFT analysis is done and the current THD of 'a' phase is shown in Fig. 4.31.

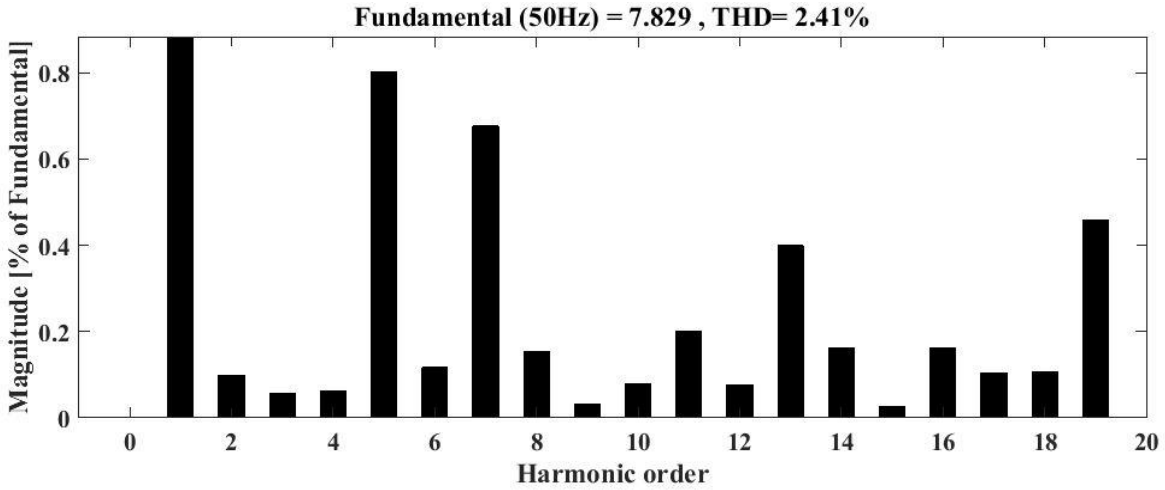


Figure 4.31: FFT analysis of phase 'a' current for the selective voltage vector based MPC.

The current THD is little higher with respect to voltage vector predictive MPC. However, it complies the IEEE 519 standards. Moreover, it reduces the iteration from 32 to 8 at each sampling time. So, the reduction of execution time is expected.

The transient response of this method is shown in Fig. 4.32 which indicates the response time for the controller to reach the reference.

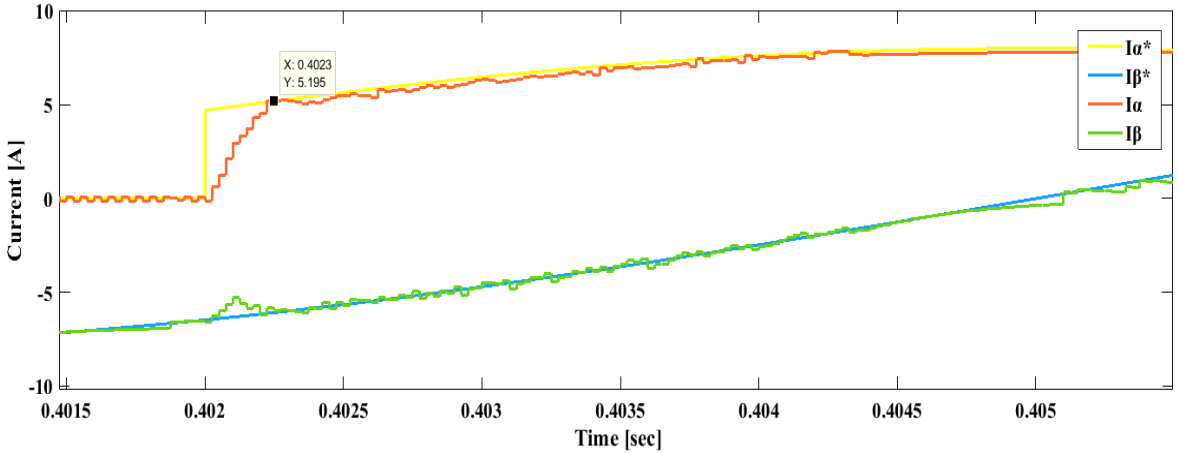


Figure 4.32: Zoomed current transient response analysis for the selective voltage vector prediction based MPC.

From Fig. 4.32, it can be seen that the transient response time of the control scheme is approximately 0.3 ms which is identical with the voltage vector prediction based MPC.

4.6 Execution time improvement analysis

The required execution time of a controller for a specific microprocessor is a vital factor for interfacing with hardware. A shorter execution time refers to better performance of a control scheme. To do so, voltage vector predictive FCS-MPC and selective voltage vector prediction based MPC methods are introduced which are already discussed in detail in the previous chapter and basic performance analysis is shown in the preceding subsection. The required execution times for the simplified MPC strategies are tested on hardware dSPACE 1104 platform. The outcomes are presented in Table 4.9.

Table 4.9: Execution time improvement using voltage predictive FCS-MPC

Control scheme	Execution time in Microprocessor (micro-sec)
FCS-MPC for NPC	37.29
FCS-MPC for SNPC	44.0
Voltage vector prediction based FCS-MPC for SNPC	34.2
Selective voltage vector based MPC for SNPC	13.8

From the Table 4.9, the proposed system is 15.25% computationally expensive than the conventional NPC inverter due to higher number of available switching states. The simplified voltage vector prediction based MPC and selective voltage vector based MPC are

computationally efficient by 8.28% and 62.9% respectively, in comparison with the conventional MPC strategy.

4.7 Summary

This chapter presents the performance of the proposed MPC based SNPC inverter system in terms of current tracking accuracy, harmonic analysis, neutral point voltage balancing, steady state and transient responses, and different loss analysis. A comparative analysis in terms of current THD, neutral point voltage balancing, transient response time and power loss has been performed with respect to the existing NPC inverter system. The quality of the injected current produced by the proposed controller meets the IEEE 519 standard. Furthermore, voltage vector prediction based MPC and selective voltage vector prediction based MPC is introduced to minimize the execution time which is a crucial factor for hardware implementation. It is shown that the execution time for the proposed system can be reduced and thus the sampling frequency can be increased, which eventually improves the output current quality.

CHAPTER V

Conclusion and Recommendations

5.1 Conclusion

Current trend of multilevel inverters (MLIs) suggest that it will bring a positive impact on the power electronics area, such as ac motor drive applications, renewable energy conversion, uninterruptable power supply (UPS) technology and so on. However, the key challenges are to select proper MLI topology with control scheme for a certain applications. A simplified version of NPC is taken for this study because SNPC comes with some inherent superior qualities such as less number of semiconductor devices which increases the reliability of the system and ease handling of capacitors voltages balancing.

The combination of inverter topology with a proper control scheme ensures better performance of a system. FCS-MPC control system is adopted as a control scheme as it offers some good qualities output namely faster dynamic response, intuitive, no need of modulation blocks etc. The proposed MPC selects an optimal control action in every sampling instant for the inverter by minimizing a predefined cost function. The cost function is designed for reducing the current tracking error, neutral point voltage variation, average switching frequency and for protecting the system from over-current. A lower average switching frequency will reduce the switching loss. The aforementioned control objectives are combined with weighting factors in the cost function. The value of the weighting factors are selected by trading-off the average switching frequency and current THD, as they are inversely related.

To analyze the performance of the proposed system, simulation has been performed using MATLAB/SIMULINK platform. Different types of analysis have been performed for the proposed 3L-SNPC inverter such as current THD analysis which has been found as 2.33% at 8.96 KHz without average switching frequency reduction. To improve the current ripple a delay compensation technique has been implemented for the FCS-MPC scheme. After delay compensation the current THD is found as 2.27% at 8.26 KHz. With considering switching frequency reduction and delay compensation, the average switching frequency is reduced to 4.51 KHz with sacrificing 0.06% current THD. The neutral point voltage variation has been found as 0.06V peak. The transient response for the SNPC inverter has been found as 0.3ms to track the reference without any overshoot. In contrast, NPC requires 0.4ms during transient to track the reference. The controller also offers decoupled control of two current components: alpha and beta components. The voltage stress has been found as maximum$\frac{V_{dc}}{2}$ volt for the load side of SNPC inverter and maximum V_{dc} for 3L-dc source side of SNPC. The common mode voltage is found in the range of $\pm\frac{V_{dc}}{3}$ volt, which is similar to the conventional NPC inverter. A comparative analysis has shown that the NPC has 1.81%

current THD at 2.46 KHz whereas for SNPC the current THD is 2.31% at 4.51 KHz average switching frequency. The average switching frequency is higher because the dc link capacitors are charged and discharged through switching of semiconductor devices.

Power loss analysis has also been performed for the proposed system. Different types of loss such as switching loss, conduction loss and harmonic loss are analyzed. For the SNPC, the switching loss, conduction loss and harmonic loss have been found as 2.8684W, 5.7179W and 0.0804W, respectively, without average switching frequency reduction. On the other hand, the losses are 1.4383W, 3.3240W and 0.0376W, respectively, for the conventional NPC. At the optimum operation point, the losses have been found as 1.5677W, 5.7117W and 0.124W, respectively. On the other hand, for the conventional NPC, they have been found as 0.4309W, 4.5763W and 0.0517W, respectively. The total loss for the SNPC is 8.667W without switching frequency reduction and 7.4034W with switching frequency reduction. Therefore, 14.57% power loss has been reduced by operating the proposed system at the optimum point. However, the overall loss for the proposed SNPC is still 46.3% higher than the conventional NPC.

Execution time of the control algorithm and thus the sampling frequency is a great concern in implementing an inverter system. The proposed MPC algorithm for SNPC inverter is computationally expensive by 15.25% than the conventional MPC algorithm for NPC inverter due to higher number of available switching states. In this research two simplified strategies are adopted: single voltage vector prediction based FCS-MPC and Selective voltage vector based MPC. It is found that the single voltage vector prediction based MPC and the selective voltage vector prediction based MPC are computationally efficient by 8.28% and 62.9%, respectively, in comparison with the conventional MPC strategy.

In conclusion, the proposed MPC based SNPC inverter yields similar performance as the conventional NPC inverter system. Due to less number of semiconductor devices used in the topology, it will enhance the system's reliability. Two capacitor voltages are well balanced, and thus the neutral point voltage variation is close to zero. The common mode voltage is similar to the conventional NPC inverter. However, the average switching frequency, voltage stress at the dc link side and overall loss are higher in the proposed SNPC inverter than the conventional NPC inverter. Hence, the proposed SNPC inverter is suitable for low power applications.

5.2 Recommendations

This work can create the following scopes for future researchers.

I. The proposed FCS-MPC based 3L-SNPC inverter system is designed and simulated in MATLAB/SIMULINK platform. Hardware implementation of the proposed 3L-SNPC inverter system will be the best way to verify the performance practically, which will be a future research scope in this area.

II. The current THD of the proposed controller still shows some small existence of different dominated harmonic components such as 5th, 7th, and 11th. Selected harmonic elimination technique may be incorporated in future with the proposed FCS-MPC, which may further improve the performance of the FCS-MPC.

III. Voltage stress across each semiconductor devices of 3L DC source portion and 2L inverter portion is not equal. So, the proposed system does not overcome it predecessor's unequal loss distribution drawbacks. More sophisticated control strategy will be implemented to overcome this problem.

IV. Common mode voltage is a crucial factor for inverter while deploying it in on-grid applications and motor driver applications. It will be considered in the cost function to reduce this voltage within an acceptable limit.

V. The main drawback of FCS-MPC such as variable switching frequency can be overcome by including a modulation block in the proposed control structure.

VI. In this study, only RL load has been considered. The proposed system can be designed for grid-connected inverter and ac motor drives applications in future.

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Publications

1. A.K. Podder, **M. Tariquzzaman**, M. Habibullah, "Comprehensive Performance Analysis of Model Predictive Current Control based On-grid Photovoltaic Inverters", *Journal of Physics* (**Accepted for Publication**).

2. M.A. Hossain, **M. Tariquzzaman**, A.K. Podder, M.S.H. Sabbir, M. Habibullah, "Predictive Current Control of a Simplified Three-level Neutral-Point Clamped Inverter", *International Conference on Electrical, Computer and Telecommunication Engineering.* (**Accepted**)