Khulna University of Engineering & Technology
B. Sc. Engineering Special Backlog Examination 2018
Department of Electrical and Electronic Engineering
EE 3113
Digital Electronics and Logic Design

Time: 3 hours | Full Marks: 210

N.B.: (i) Answer **ANY THREE** questions from each section in separate scripts.
(ii) Figures in the right margin indicate full marks.

Section A

Q1. (a) Write down the significance of using complement's in digital system. Determine the base and missing number "*" for the following subtraction. (08)

$$(5162 - 2644) = 2*15$$

(b) Represent the number $3113)_{10}$ in the following codes, (i) BCD, (ii) 2421, (iii) Excess-3. (06)

(c) Explain the minimization technique using Quine-Mcclusky method. Determine the prime implicants for the following function: (12)

$$F(A, B, C, D, E) = \sum(0,2,5,8,26,30) + \sum_{d}(10,12,24)$$

(d) What are the performance indices of digital IC's? Explain them clearly. (09)

Q2. (a) Mention the differences between MUX and encoder. Implement the function, $F(A,B,C,D) = \prod(0,5,6,8,13,14)$ using MUX. (10)

(b) Implement, F = AB + CD + E using NAND gate only. (07)

(c) Let $f = \sum(5,6,13)$ and $f_1 = \prod(4,7,12,14,15)$. Determine f_2 such that $f = f_1 f_2'$. (09)

(d) Express the following switching circuit in binary logic notation. Also implement by NOR gate using b (09)

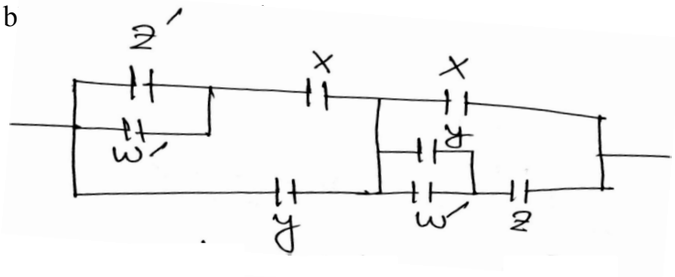

Figure for Q2(d)

Q3. (a) What is meant by ROM? Draw the logic construction of a 32×4 ROM. Design a BCD to Excess-3 code converter circuit using ROM. (14)

(b) What is meant by PLD? Show the comparison among PLA, PROM and PAL. Implement the following functions using PAL. (15)

$W(A,B,C,D) = \sum(0,2,6,7,8,9,12,13)$
$X(A,B,C,D) = \sum(0,2,6,7,8,9,12,13,14)$
$Y(A,B,C,D) = \sum(2,3,8,9,10,12,13)$
$Z(A,B,C,D) = \sum(1,3,4,6,9,12,13,14,15)$

(c) How can the fan out of DTL gate be increased? (06)

Q4. (a) Express $F(A,B,C,D) = B + \bar{C}$ in POS form and also implement the function using ROM. (12)

(b) What are the differences between ROM, PAL and PLA? Implement the following function using PLA. (12)

$F_1(A,B,C) = \prod(0,1,3,5)$ and $F_2(A,B,C) = \prod(0,3,4,5)$

(c) Explain the significance of using parity bit in digital system. Design an odd parity checker circuit for 3-bit system. (11)

Section B

Q5. (a) What is latch? What are the features of edge triggering flip flop? (08)

(b) How can you use a T-FF as a pulse frequency divider? How can a chain of T-FF be used as counter? (09)

(c) Design a sequential circuit that has 3 FFs A, B and C, one input *x* and one output *y*. The circuit is to be designed by treating the unused states as don't care conditions. Use JK FFs in your design by considering the state diagram as shown in Fig. Q5(c). (12)

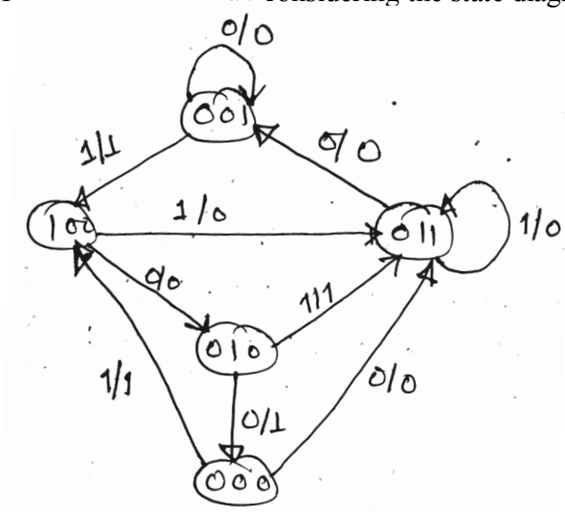

Figure for Q5(c)

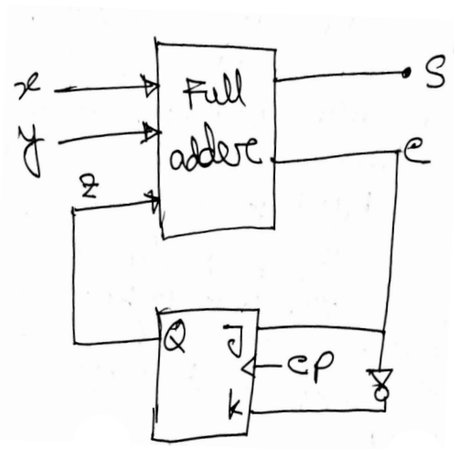

Figure for Q7(d)

(d) Write the Verilog code for full subtractor. (06)

Q6. (a) What are the benefits of state reduction? What can be achieved with proper state assignment? (06)

(b) Design a counter with repeated binary sequence 0, 1, 2, 4, 6. Use T Flip-flops. (10)

(c) The content of a 4 bit shift register is initially 1110. The register is shifted 6 times to the left with the serial input being 101101. What is the content of the register after each shift? (05)

(d) Design a serial 2's complementer. Use JK flip flop. (14)

Q7. (a) Explain why we use both RAM's and PROM's in a system. (06)

(b) How data is written into and read from magnetic core type memory. (09)

(c) What is race-around condition? How can it be overcome? Explain clearly. (09)

(d) Draw the state diagram for the circuit shown in Fig. Q7(d). Also find the state equation. (11)

Q8. (a) Given the 11-bit data word 11001001010, generate the 15 bit Hamming code word. (10)

(b) Write a user defined primitive for a two input MUX in Verilog HDL. (08)

(c) Draw the block diagram of a D/A converter. How does R-2R ladder network work as D/A converter? (10)

(d) What is FPGA? Draw the block diagram of FPGA architecture and describe its operation. (07)