IMPLEMENTATION OF MICROCONTROLLER BASED ASYMMETRIC THREE-LEVEL SINGLE-PHASE INVERTER

by

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A project submitted in partial fulfillment of the requirements for the degree of Master of Science in Engineering in Electrical & Electronic Engineering Department

Khulna University of Engineering & Technology

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December, 2010

Declaration

This is to certify that the project work entitled "*Implementation of Microcontroller Based Asymmetric Three-Level Single-Phase Inverter*" carried by Abdulla Ibna karim in the Department of Electrical and Electronic Engineering, Khulna University of Engineering & Technology, Bangladesh. The above project work or any-part of the work has not been submitted anywhere for the award of any degree or diploma.

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ACKNOWLEDGEMENTS

First and foremost, all praises for Allah who has given me all the help, guidance, and courage to finish my project work. May Allah help me to convey all what I learned for the benefit.

I am so thankful to my thesis supervisor A.N.M. Enamul Kabir and co-supervisor Dr. Md. Abdur Rafiq, for their continuous help and guidance throughout the project. As my project advisor, A.N.M. Enamul Kabir have given every possible effort to help me to achieve my goals. Working with him is an experience that I never forget in my life. I am also thankful to Professor Dr. Md. Rafiqul Islam, Mr. Mohd. Noor Islam, Dr. Mohiuddin Ahmad for their help and suggestion.

I would also like to thank Mrs. Mamataz Begum, my mother, the rest of my family, especially my father, brother, and sister, as well as my friends for their continued support. Also, I want to thanks Mr. Nazmul Haque technicians of Hardware lab for constructing the apparatus. I also appreciate the efforts and advice put on by the Hardware laboratory personnel.

The work presented in this project would not have been possible without the support of the Khulna University of Engineering & Technology Administration, under the grant my proposal to Electrical and Electronic Engineering department. Finally, we would like to thank all whose direct and indirect support helped us completing my project in time.

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ABSTRACT

Switching-mode single-phase DC-AC inverters have been widely used in many applications such as AC motor drivers and uninterrupted power supply systems. Among various control techniques, microcontroller based control is the most effective one generally used to regulate the magnitude as well as frequency of the converter's output voltage. In this project, an open-loop asymmetric three-level inverter with a microcontroller based control approach is established. This novel topology with a microcontroller based control approach has advantages of low voltage device, less harmonics and power loss, and more flexible device selection, compared with conventional single phase H-bridge inverter and NPC inverter. Theoretical analysis is discussed in this report. Experimental implementation based on microcontroller is also performed and the results are demonstrated in this project.

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NOMENCLATURE

ATLI	Asymmetric Three-Level Inverter
CSI	Current Source Inverter
EMI	Electrical Magnetic Interference
IGBT	Insulated Gate Bipolar Transistor
PWM	Pulse Width Modulation
THD	Total Harmonics Distortion
VSI	Voltage Source Inverter
AC	Alternating Current
DC	Direct Current

CHAPTER 1

INTRODUCTION

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1.1 Introduction

Most electronic appliance users know from experience that electrical power supply from the mains is not reliable. All over the world there is significant electrical power supply interruptions which are common after hurricane or severe storm. Also there is increase in occurrence of power supply disturbance, which can be viewed as a form of power pollution. High voltage spikes and momentary voltage drops are therefore common. These power supply disturbances may affect the performance of sensitive equipment in private and corporate organisations causing critical loss of data and even damage to equipment.

The supplies that should be available for use as recommended by the Institute of Electrical Engineers (IEE) should be continuous, uninterrupted, with constant frequency and within the load demand in terms of voltage and current. These requirements have become even more relevant in view of the high sensitivity and sophistication of modern technological equipment in use today.

In Bangladesh power today off and poor quality power supply are the order of the day. A wide range of factors have been identified for this problem. They include natural disasters, vandalism, maintainability and sustainability inadequacies, lack of local content, and absence of integrated and collaborated capacity building programme. The problem of poor quality power supply can not be properly addressed without a review of other factors such as lack of political will to invest adequately in power sector, absence of replacement policy resulting in obsolete equipment, unsustainable human capacity building, and inadequate reward and remuneration system to motivate human resources team to perform well.

The progress made in developing alternative sources of energy over the last decades has shown that independent power system (those using sources other than fossil fuels) are not only possible but are also very practical. In fact a wide variety of generating equipment is now available to allow individuals take advantage of just any renewable sources of energy. For a number of reasons however most of these systems produce only direct current (DC), and often do so only at low voltages. Nonetheless it is generally agreed that the greatest potential use for alternative energy in the future will be to serve alternating current (AC) loads, since these exist in the vast majority of homes.

The two types of electricity; direct current and alternating current, each has its advantages and disadvantages, and most types of devices will only run on one or the other. Therefore, it is useful to be able to change electricity from one form to the other. The process of changing AC into DC is called conversion. Devices that perform this process are called converters. Changing DC into AC is the opposite process and is called inversion. A device that does this is called an inverter.

Most people use converters on a daily basis even if they don't realize it, while inverters are used only for special applications. This is because most people have AC power in their houses and therefore have little need for a device that creates AC from a DC source. However, inverters are useful for a wide range of applications, including letting we run small 220V AC household appliances from car battery or electrical system, which is DC. In the DC world, inverters are a major component in uninterruptible power supplies, changing stored battery energy into a form AC-powered DC power supply can use.

1.2 Literature Review

In recent years, many places in the world have been experiencing continued shortage of electric power or energy crisis due to their fast increasing demand [1]-[2]. To solve this problem, significant efforts of research and development have been given in two areas: Firstly, improve the efficiency of present power conversion process and utilization system. This is possible due to the confluence of several factors:

(1) The fast development of the power semiconductor devices, converters and inverters. Various high power semiconductor devices, such as Isolated Gate Bipolar Transistors (IGBT) and power MOSFET were developed and become commercially available. Nowadays, the increased power ratings as well as switching speed, ease of control, and reduced costs of power semiconductor devices make the new inverter topologies possible [1].

(2) The rapid advancement of microprocessors. The controller for a power inverter requires a high controlling and data-processing speed to achieve high performance. The speed of microprocessors has been raised dramatically in last 15 years. Todays microprocessors are operating at a data-processing rate of up to megahertz, which can meet the requirements of high-performance control, thus making the real-time digital control of power converter realizable.

Secondly, development of efficient renewable energy generation and conversion systems to supplement conventional fossil-fuel based energy supply and eventually replace it.

Todays power conversion topologies can be divided into four categories according to the input and output power forms: AC-DC converter (rectifier), DC-AC converter (inverter), DC-DC converter (Chopper) and AC-AC converter (Cyclo Converter) [3]. Each type of converter has its specific application field. In ac motor drives, an uninterruptible ac power supplies have to produce a sinusoidal ac output with controllable magnitude and frequency. The switch-mode DC-AC converters are used [4-6] for this purpose. If the input to converter is a dc voltage source, the converter is referred to as voltage source inverter (VSI); if the input to converter is a dc current source , the converter is referred to as current source inverter (CSI) which is used only for very high power ac motor drives [6]. In this project, only VSI will be introduced due to its wider application. The inverters can also be divided into single-phase converters and three-phase converters. In this project single-phase asymmetric inverter is employed for discussion. Asymmetric three-level inverter (ATLI) consists of one H-bridge arm and one neutral point clamped (NPC) inverter arm.

The topology has two important advantages that make it well suited to this market: less harmonic component than traditional two-level input and lower voltage rating on the main switching

devices [7-8]. However, it also has disadvantages compared with the H-bridge inverter. Because it uses twice as many switches, the cost for the whole inverter increases accordingly. To get the highest performance-to-cost ratio, an asymmetric three-level inverter (ATLI) is developed. The control scheme of asymmetric three-level inverter (ATLI) is generated using microcontroller in this project. Microcontroller have many advantage such as it has less complexity , lower in price, lower power loss etc. Using microcontroller it is also possible to control the output frequency. In general there are two ways, direct generation and indirect generation to generate the gate pulse using microcontroller. From those two methods the simplest one is choosen in this project to generate the gate pulse for asymmetric three-level inverter (ATLI).

1.3 Objective of this project

The objectives of this project are as follows,

a) Using microcontroller gate pulse generation in direct method to drive the IGBT.

b) Controlling the output frequency of asymmetric three-level inverter (ATLI) by using microcontroller.

c) To construct the asymmetric three-level inverter (ATLI) circuit topology

d) The generated gate pulse using microcontroller then use it in the control scheme for ATLI circuit topology.

1.4 Project organization

This project report consists of seven chapters with chapter 1 presenting the background information. The motivation for conducting this project is discussed as well as main objectives.

In chapter 2, an overview of power inverter technologies is given here. Different type of inverters and their operation are also given in this chapter.

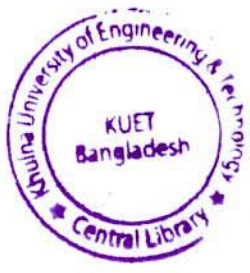
In chapter 3, an asymmetric three-level dc-ac converter and improved innverter topology are discussed. The circuit topology of the power inverters will be discussed and selected in details. It will describe and analyze the circuit configuration and operation as well as PWM control method.

In chapter 4, the Microcontroller and its internal configuration is focused. The overview of 8051 microcontroller, internal architecture, memory space allocation and assembling and running an 8051 program is also given in this chapter.

In chapter 5, a Microcontroller based control configuration and program design of gate pulse generation will be discussed. Also in this chapter different techniques of gate pulse generation using microcontroller will be discussed.

In chapture 6, the hardware implementation of open-loop ATLI is shown. An experimental prototype will be presented. A Microcontroller based control will be discussed. Finally, the experimental results will be included and discussed

In chapter 7, conclusion and an outlook on the future development of this project is given here. The references and appendix will be attached at the end of this thesis.



CHAPTER 2

INVERTER

2.1 Introduction

DC-AC converters are known as inverters. The function of an inverter is to change a dc input voltage to symmetric AC output voltage of desired magnitude and frequency. For this reason it is also called frequency converter. Power inverters produce one of three different types of wave output:

- Square Wave
- Modified Square Wave (Modified Sine Wave)
- Pure Sine Wave (True Sine Wave)

The three different wave signals represent three different qualities of power output and consequently, three different price categories. Square wave inverters result in uneven power delivery that is not efficient for running most devices. Square wave inverters were the first types of inverters made and are obsolete.

Modified square wave (modified sine wave) inverters deliver power that is consistent and efficient enough to run most devices fine. This type of inverter is probably the most popular. Pure sine wave inverters are the most expensive, but they also deliver the most consistent wave output. Some sensitive equipment requires a sine wave, like variable speed control motor. The output voltage could be fixed or variable at a fixed or variable frequency. A variable output voltage can be obtained by varying the input dc voltage and maintaining the gain of the inverter constant. On the other hand, if the dc input is fixed and it is not controllable a variable output voltage can be obtained by varying the gain of the inverter, which is normally accomplished by pulse width modulation (PWM). The inverter gain may be defined as the ratio of the ac output voltage to dc input voltage. If input voltage of an inverter remains constant it is called VFI (Voltage fed inverter) and when current remains constant it is called CFI (Current fed inverter).

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Figure 2.1 Basic outlook of inverter

2.2 Basic design

In one simple inverter circuit, DC power supply is connected to a Transformer through the centre tap of the primary winding. A switch is rapidly switched back and forth to allow current to flow back to the DC source following two alternate paths through one end of the primary winding and then the other. The alternation of the direction of current in the primary winding of the transformer produces alternating current (AC) in the secondary circuit.

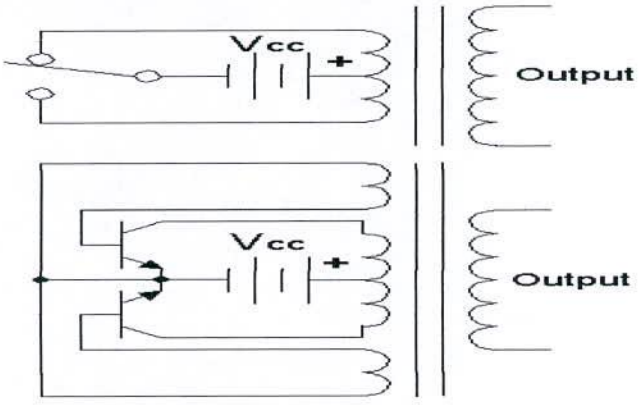

Figure 2.2 Simple inverter circuit shown with an electromechanical switch and automatic equivalent auto-switching device implemented with two transistors and split winding auto-transformer in place of the mechanical switch.

2.3 Output waveform

The switch in the simple inverter described above produces a square voltage waveform as opposed to the sinusoidal waveform that is the usual waveform of an AC power supply. Using Fourier analysis, periodic waveforms are represented as the sum of an infinite series of sine waves. The sine wave that has the same frequency as the original waveform is called the fundamental component. The other sine waves, called harmonics, that are included in the series have frequencies that are integral multiples of the fundamental frequency.

The quality of the inverter output waveform can be expressed by using the Fourier analysis data to calculate the total harmonic distortion (THD). The quality of output waveform that is needed from an inverter depends on the characteristics of the connected load. Some loads need a nearly perfect sine wave voltage supply in order to work properly. Other loads may work quite well with a square wave voltage.

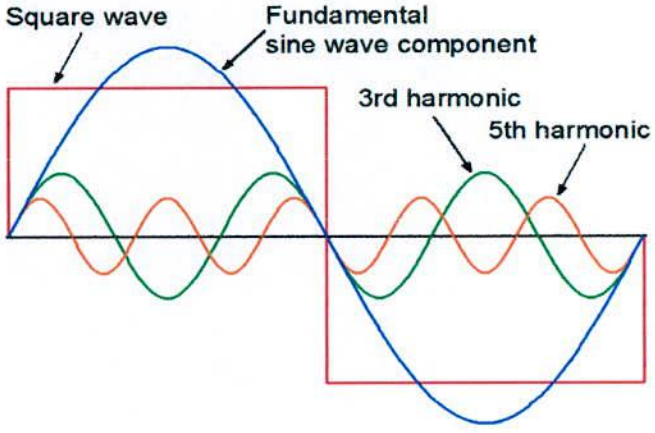

Figure 2.3 Square waveform with fundamental sine wave component, 3rd harmonic and 5th Harmonic.

2.4 Types of Inverter

Inverters can be broadly classified into two types according to phase:

(1) Single phase inverters and
(2) Three phase inverters.

Inverters can be broadly classified into three types according to input voltage and current:

(1) Current fed inverter (CFI)
(2) Voltage fed inverter (VFI)
(3) Variable dc linked inverter

2.4.1 Single phase inverter

Single-phase inverters are widely used in industrial applications such as induction heating, standby power supplies and uninterruptible supplies. A block diagram representation of a single-phase inverter is given in Fig.2.4. The inverter consists of two switching devices (represented as ideal switches) connected in the form of a bridge.

Single phase half bridge inverter:

- Consists of 2 choppers, 3-wire DC source
- Transistors switched on and off alternately
- Need to isolate the gate signal for Q1 (upper device)
- Each provides opposite polarity of Vs/2 across the load

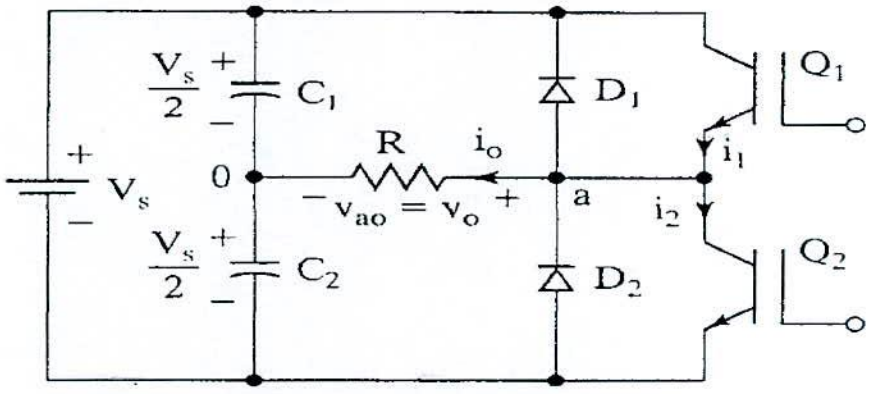

Figure 2.4 Single phase inverter

Operational details:

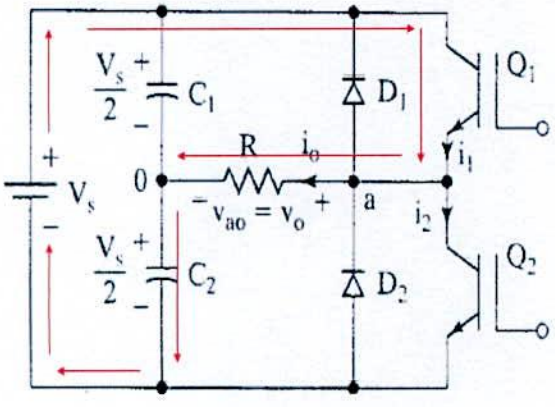

Figure 2.5 Mode 1-Q1 on and Q2 off

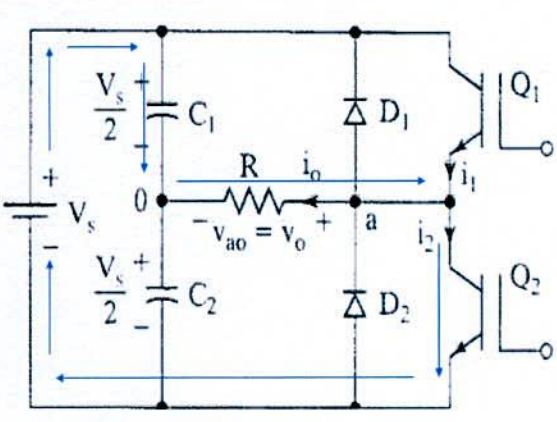

Figure 2.6 Mode 1-Q2 on and Q21off

The principle of operation of a single-phase inverters can be explained with Figure 2.5 & 2.6.The inverter circuit consists of two choppers. When only transistor Q_1 is turned on (See figure 2.5) for a time $T_0/2$,the instantaneous voltage across the load v_0 is $V_s/2$. If transistor Q_2 only is turned on (See figure 2.6) for a time $T_0/2$, - $V_s/2$ appears across the load. The logic circuit should be designed such that Q_1 and Q_2 are not turned on at the same time.

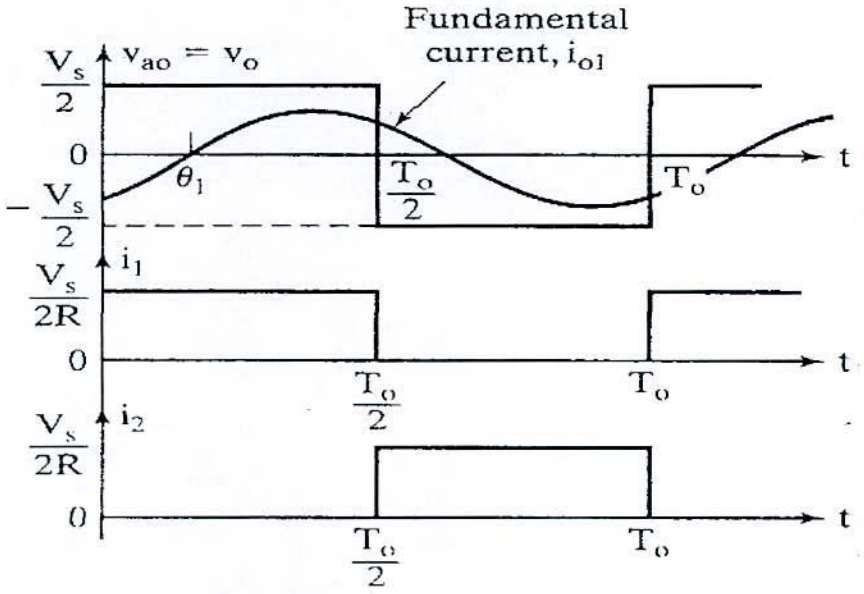

Figure 2.7 Waveforms with resistive load

Single phase full bridge inverter:

- Consists of 4 choppers and a 3-wire DC source
- Q1-Q2 and Q3-Q4 switched on and off alternately
- Need to isolate the gate signal for Q1 and Q3 (upper)
- Each pair provide opposite polarity of Vs across the load

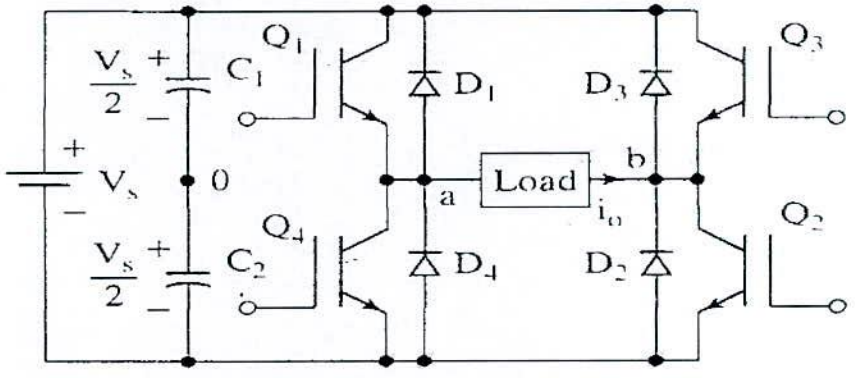

Figure 2.8 Single phase full bridge inverter

Operational details:

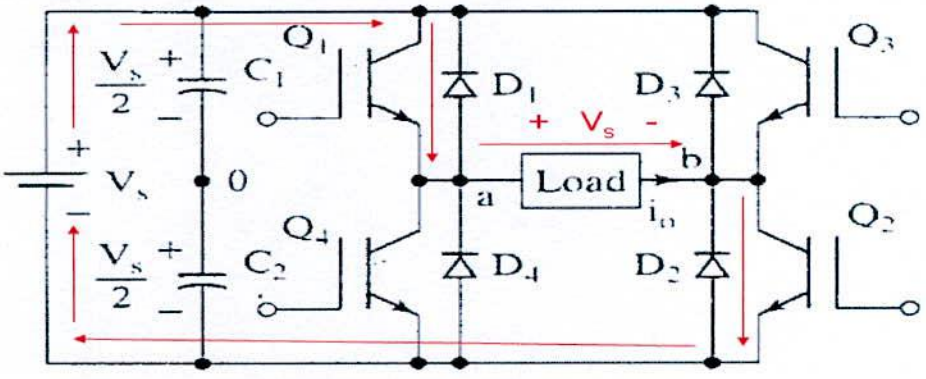

Figure 2.9 Q1-Q2 on, Q3-Q4 off, vo = Vs

A single-phase full bridge inverter is as shown in figure 2.8.It consists of four choppers. When transistor Q1 and Q2 are turned on (See figure 2.9) simultaneously, the input voltage V_s appears across the load.

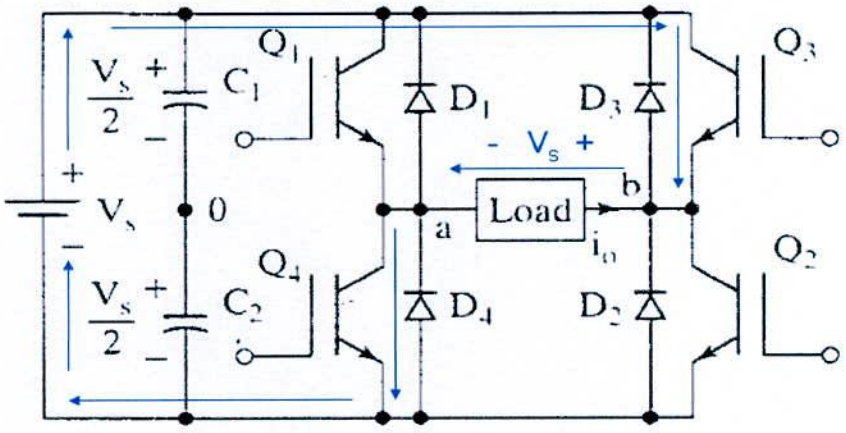

Figure 2.10 Q3-Q4 on, Q1-Q2 off, vo = -Vs

If transistor Q3 & Q4 turned on (See figure 2.10) at the same time , the voltage across the load is reversed and is - V_s.

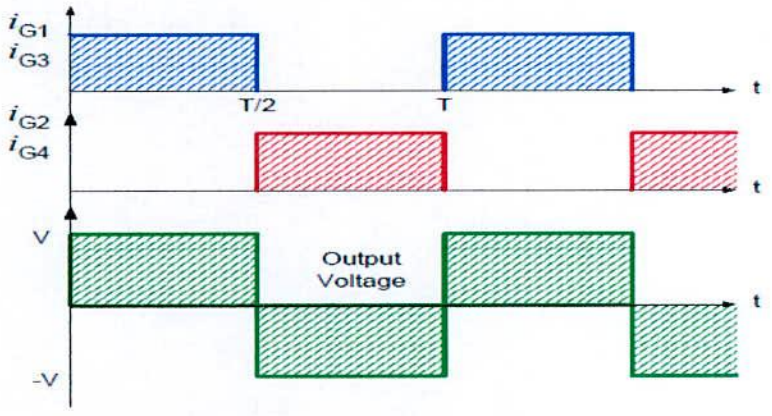

Figure 2.11 Waveforms of full bridge inverter

2.4.2 Three phase inverter

The standard three-phase inverter has as its genesis, the hex-bridge. The hex-bridge takes a DC bus voltage and uses six switches (MOSFETS) arranged in three phase legs as shown in Figure 2.12. Each line is then connected from the middle of each phase leg to the motor itself. The waveforms on these lines must be a balanced three-phase sinusoidal waveform in order to drive the induction motor properly. This is achieved by carefully controlling the switching waveforms at the gates of the switches. For each leg, the two switches have a 50% duty cycle ensuring that there will be no DC component in the output signal.

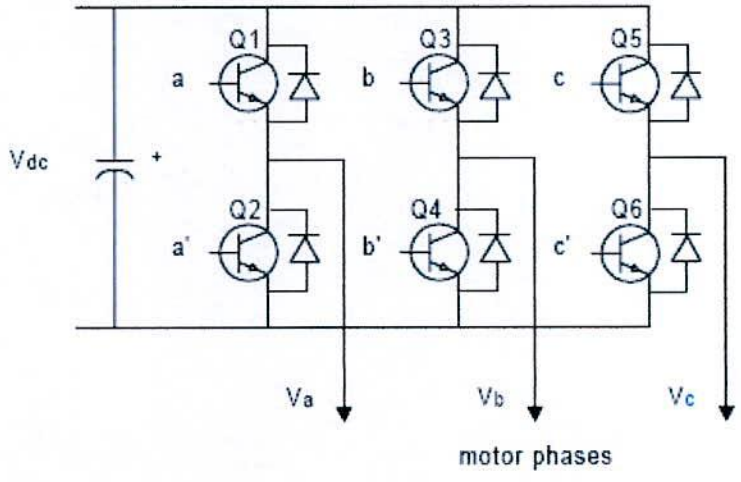

Figure 2.12 Three phase inverter

There are two kinds of switches that were considered for this range of power applications, Insulated Gate Bipolar Transistors (IGBTs) or MOSFETs. To meet the project specifications, the switch needed ratings of 400V and 10A. In addition, the project needed a switch which minimized losses; therefore, switches with lower on-state resistance are desirable. The IGBT considered for this design was the HGTP12N60B3D, which has a small equivalent resistance of approximately 0.07Ω, but IGBTs also have a voltage drop at all times due to the collector-emitter saturation voltage, which in this case is equal to 1.7V. The MOSFET investigated was the FQP17N40, which has an on-state resistance of 0.27Ω.

The power losses of the IGBT and the FET are plotted against the current are shown in figure 2.13. The IGBT has a fairly linear loss curve because the loss is mostly due to the IVsat, while the MOSFET losses are due to the $I^2R_{DS(on)}$. The MOSFET losses increase faster with current, but the MOSFET losses do not surpass the IGBT losses until current is approximately greater than 9A. The motor used in our project is rated for 3A so the current will most likely operate in the ranges most likely conducive to MOSFET implementation.

In addition to having smaller losses in our operating region, the FQP17N40 is cheaper. It is $0.96 in a quantity of 1000, while the HGTP12N60B3D is $1.70 in the same quantity. The HGTP12N60 is rated for 600V, which is the very low end of IGBT ratings. IGBTs are usually used in higher power applications, so this part is not extremely common. The savings in losses and price prompted us to choose the FQP17N40 as the switch to be implemented in the hex-bridge.

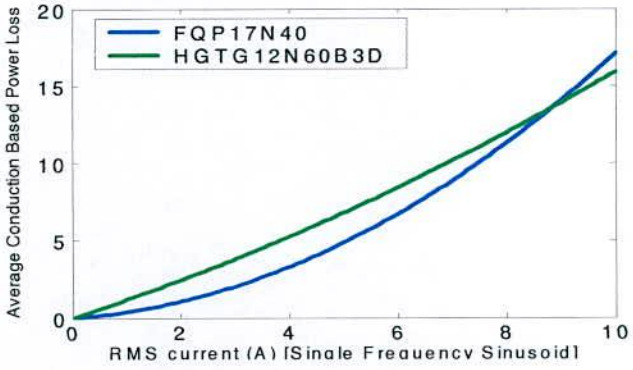

Figure 2.13 Power losses in IGBT vs. FET

2.4.3 Current Fed Inverter

Current source inverters are well-known for ac motor drives. The most widely used CSI would be the auto sequentially commutated inverter (ASCI) shown in Fig. 2.14.The ASCI has many advantages such as ruggedness, fuse less protection, full four-quadrant operation, etc. However, ASCI also has quite a few shortcomings, such as

1) large high-voltage capacitors,

2) high-voltage thyristors and power diodes,

3) high-voltage motor terminal stresses,

4) limited range of operating frequency, etc.

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Thus the ASCI is usually designed by compromising high voltage stresses and operating range. In spite of such limitations, the ASCI has been preferred simply because there were no other CSIs comparable to the ASCI. In this project a new CSI which is believed to be much more advantageous than the ASCI is proposed. The new CSI, which is called the simultaneous recovery and commutation inverter (SRCI), operates in a much wider frequency range with much lower voltage stress on the motor terminals and the power devices. The SRCI has smoother current waveforms, and furthermore it can be built with considerably lower cost than the ASCI.

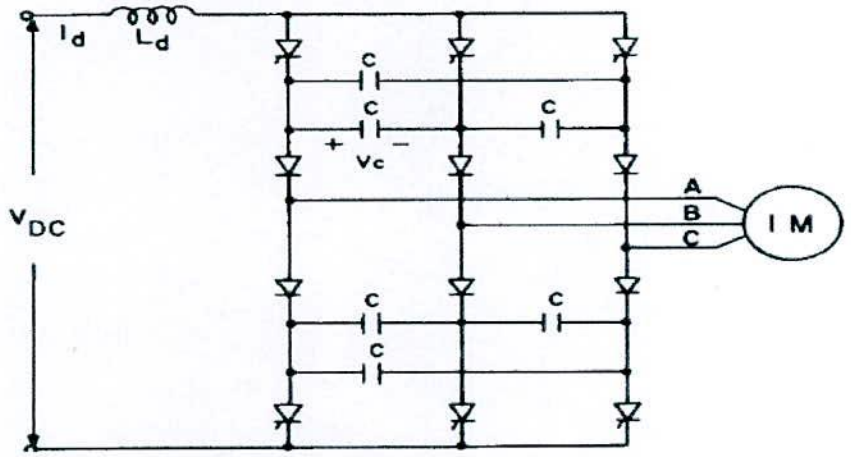

Figure 2.14 ASCI inverter.

2.4.4 Voltage Fed Inverter

The schematic diagram of a four-leg inverter is shown in Fig. 2.15. This topology is known to produce balanced output voltages even under unbalanced load conditions[9]. Due to the additional leg, a four-leg inverter can assume sixteen topologies which is twice the number of topologies a conventional three-leg inverter can assume[10]. These topologies are shown in Fig. 2.16 & 2.17. The topologies are similar to the three-leg inverter with the fourth leg being connected either to the negative rail (figure 2.16) or to the positive rail (figure 2.17). Each of these topologies is referred to as a switching state. Thus a four-leg inverter can produce sixteen switching states.

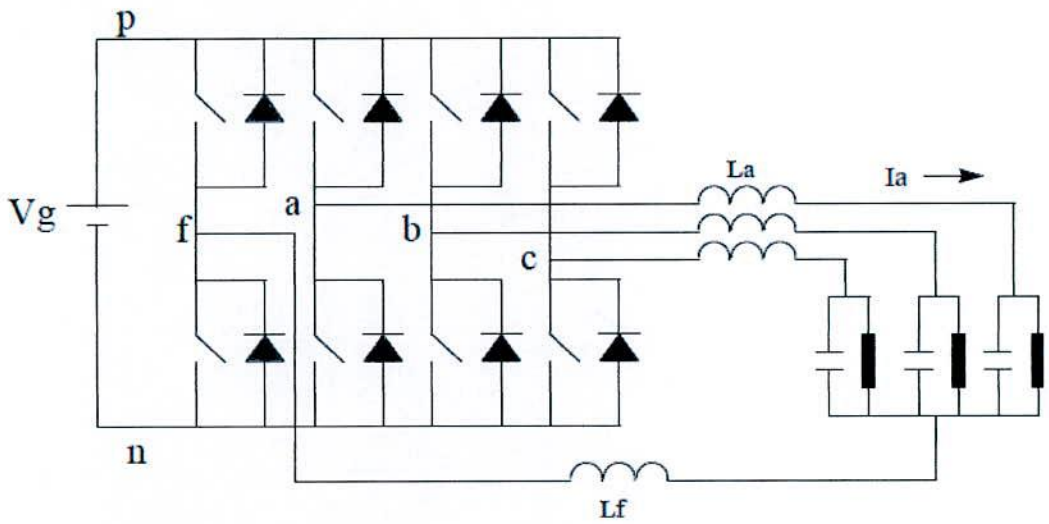

Figure 2.15 Topology of a four-leg voltage source inverter.

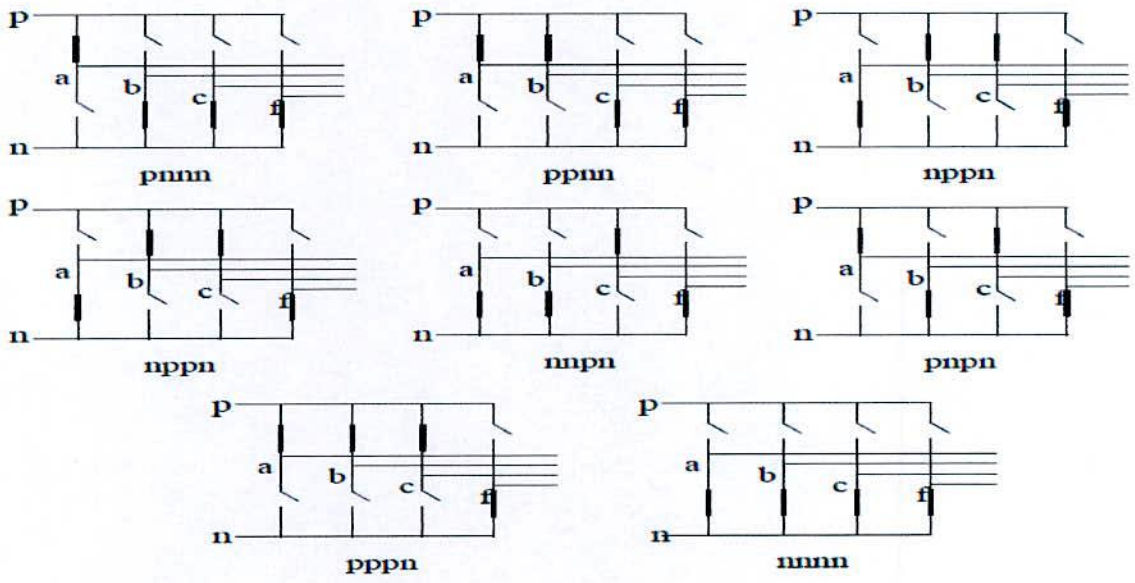

Figure 2.16 Topologies of a four-leg voltage source inverter.

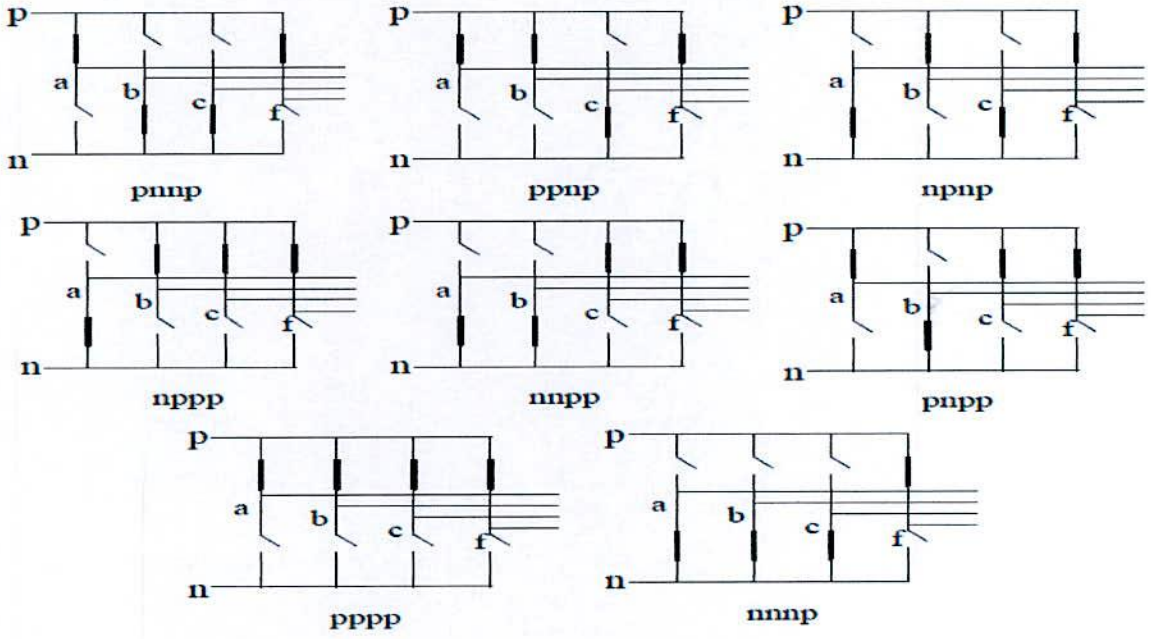

Figure 2.17 Topologies of a four-leg voltage source inverter.

CHAPTER 3

ASYMMETRIC THREE-LEVEL DC-AC INVERTER

3.1 Introduction

The basic concept of DC-AC converters are discussed in Chapter 2. In single-phase applications, what the project is especially interested about the quality of the output voltage that supplies to the load.It is expected the converter can supply a desired sinusoidal voltage output with lower harmonics or total harmonic distortion (THD). Besides the THD, it require a proper positioning in the frequency domain of the output voltage harmonics. The low frequency or low order harmonics are undesired since a bulky and expensive LC filter is needed to reduce or eliminate these harmonics. As mentioned in Chapter 2, the most-widely used single-phase DC-AC converter is H-bridge inverter. However, this H-bridge circuit produces high harmonic content in the output voltage since the output is in a two-level waveform. Better waveform and voltage control quality can be obtained by advanced inverter topologies.

3.2 Power Converter Technology Overview

A single-phase H-bridge inverter is shown in Figure 3.1.

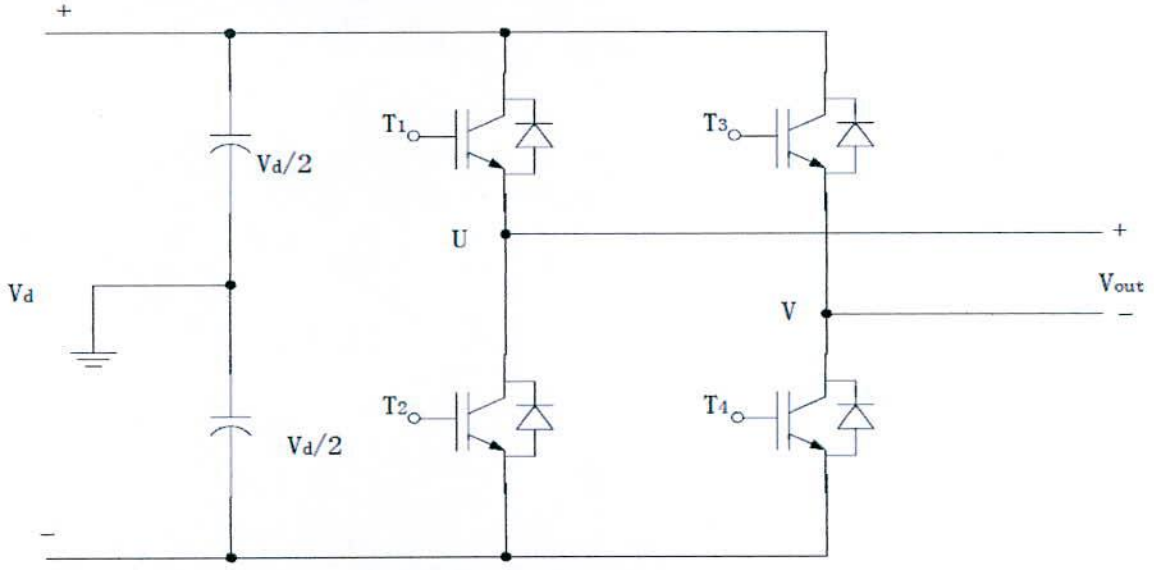

Figure 3.1 Single-phase H-bridge

The H-bridge topology inverter is the most popular single-phase converter in various applications, especially in higher power rating applications. It consists of two arms and outputs a single-phase AC output voltage, V_{out} to the load. Pulse Width Modulation (PWM) techniques [5-6],[11] are used to control the switching devices on and off. During last few years, PWM technique has been the subject of intensive research and a large variety of PWM control schemes have been discussed. Among them, sinusoidal, hysterieiss, and space-vector implementations are most commonly used [11]. Sinusoidal PWM (SPWM) approach is often used in single-phase applications.

3.2.1 Asymmetric Three-Level Inverter Topology

A three-level Neutral Point Clamped (NPC) inverter [7] is shown in Figure 3.2.

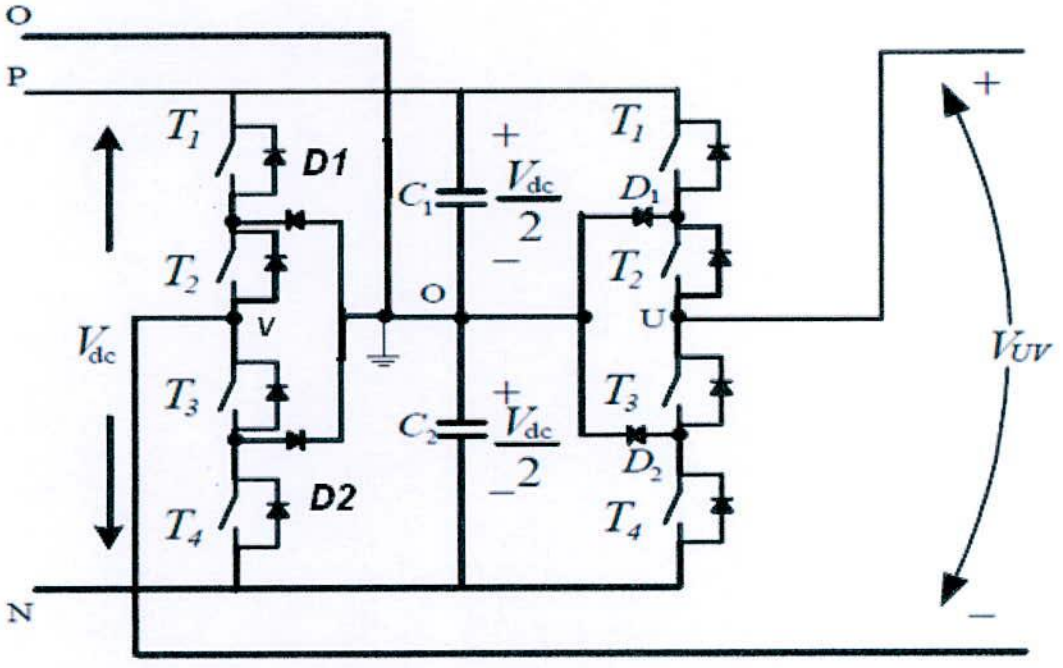

Figure 3.2 Neutral Point Clamped (NPC) inverter

Different from an H-bridge inverter, each arm of NPC inverter consists of 4 power semiconductor switching devices T1-T4 as well as two clamping diodes D1 and D2. Among

them, T1 and T3 are a complementary switching pair, i.e. when T1 is on, T3 is off; when T1 is off, T3 is on. Similarly, T2 and T4 is another complementary switching pair. The inverter is capable of connecting the load to positive DC bus (when T1 and T2 are both switched on), the negative DC bus (when T3 and T4 are both switched on) and the DC bus neutral point (when T2 and T3 are both switched on). The operating states are summarized and given in Table 3.1.

Output Voltage V_{an}	State of Switches			
	T_1	T_2	T_3	T_4
$V_{dc}/2$	1	1	0	0
0	0	1	1	0
$-V_{dc}/2$	0	0	1	1

Table 3.1 Arm-to-neutral point output voltage in different switch conditions

Therefore, the output voltage has three levels: Vdc/2, 0 and –Vdc/2. This type of inverter is commonly used for high voltage applications. The topology has two important advantages that make it well suited to the local market: less harmonic component than traditional two-level input and lower voltage rating on the main switching devices [7-8]. However, it also has disadvantages compared with the H-bridge inverter. Because it uses twice as many switches, the cost for the whole inverter increases correspondingly. To get the highest performance-to-cost ratio, an asymmetric three-level inverter (ATLI) is developed. The topology of ATLI is shown in Figure 3.3. This ATLI consists of one H bridge arm and one NPC three-level arm. The inverter circuit, control and application in a solar power system will be further developed and evaluated in details in this project work.

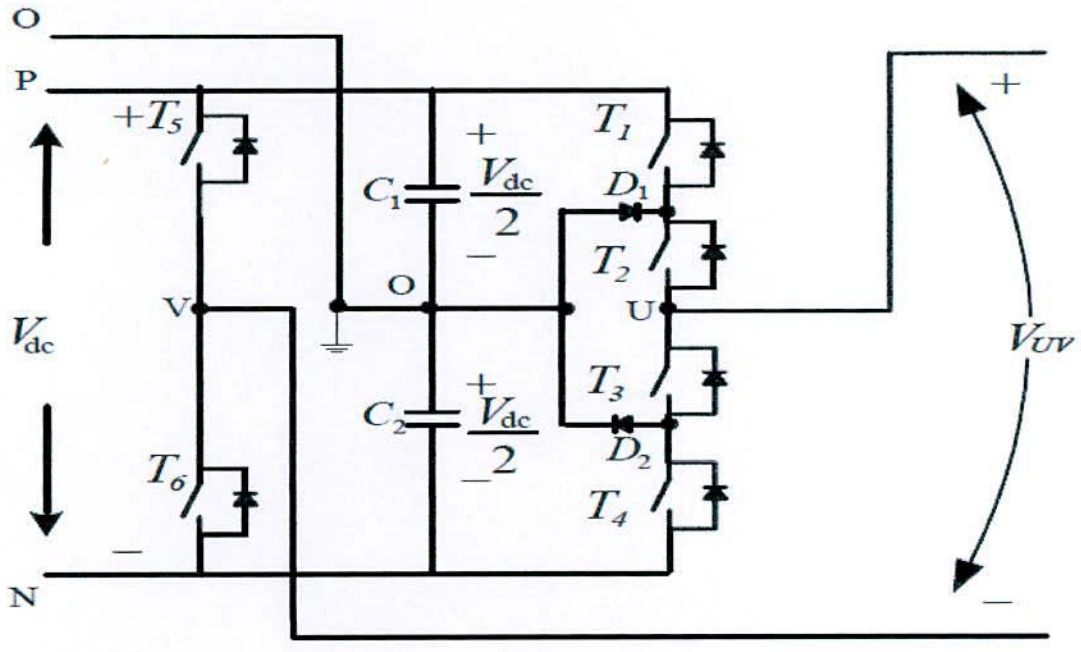

Figure 3.3 Asymmetric three-level inverter

3.2.2 Modulation Approaches for Asymmetric Three-Level Inverter

As shown in Figure 3.3, the asymmetric three-level inverter (ATLI) consists of one H bridge arm and one NPC three-level arm. The operation principle of the H-bridge arm and the operation of an NPC three-level arm are last section respectively. In this section, the control method for this new hybrid inverter will be discussed in detail. A control method of sinusoidal pulse-width modulation (SPWM) can be employed in SPWM control scheme in order to generate a sinusoidal AC output with the desired magnitude Vm and frequency f1. For NPC converter arm, SPWM technology is still employed. However, considering two pairs of complementary switching devices in each arm, two sets of carriers or two control signals with different phases should be used. Two different SPWM schemes for three-level converter arm are shown in Figure 3.4 and Figure 3.5.

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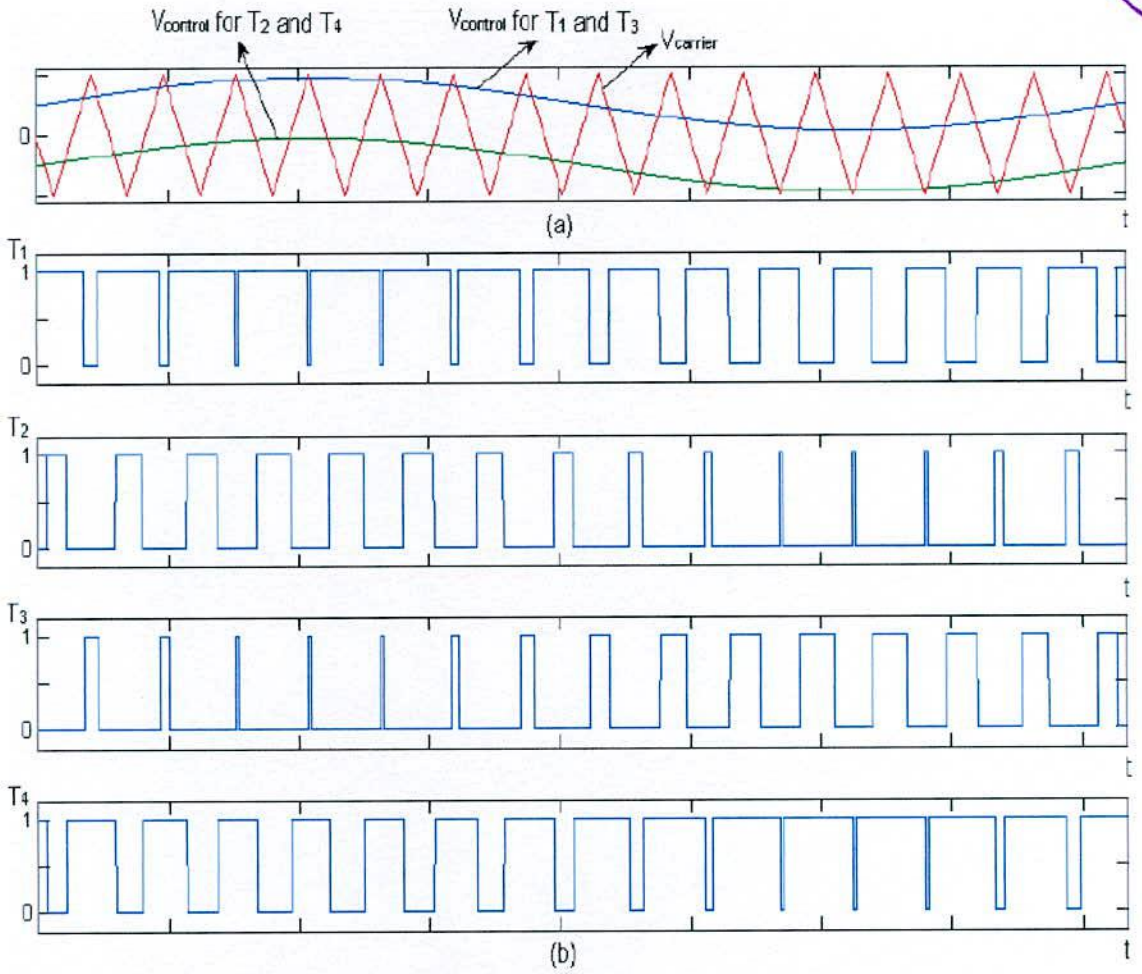


Figure 3.4 Dipolar PWM scheme and gate pulse waveforms generated

The PWM scheme in Figure 3.4 (a) employs two control signals, as in unipolar PWM scheme [12]. Each Control signal controls the switching of one pair of complementary switching devices. The top sinusoidal control signal is for T_1 and T_3 while the bottom sinusoidal control signal is for T_2 and T_4. Figure 3.4 (b) shows the switching signals for T_1- T_4. In another PWM scheme in Figure 3.4, only one control signal is involved, but two carrier signals are employed [5]. The top triangular carrier signal is for T_1 and T_3 while the bottom triangular carrier signal is for T_2 and T_4. Figure 3.5 shows the another control switching signals for T_1- T_4.Either of these two PWM schemes can be used for NPC converter arm, in which case the bipolar PWM approach should be employed for H-bridge arm.

However, they would not be the optimal PWM schemes for asymmetric three-level inverter, because in either case, switching devices in both arms switch at carrier's frequency which is relative high, thus the switching loss will be high.

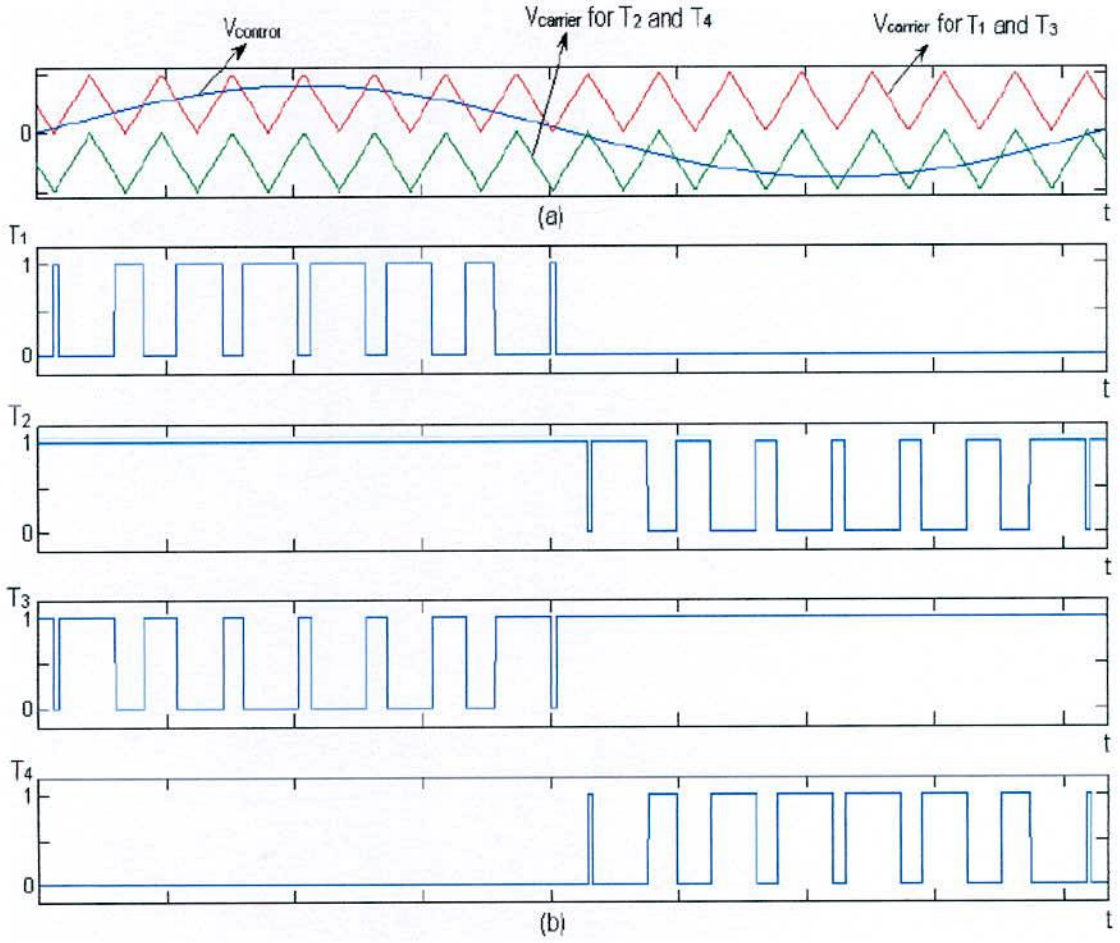
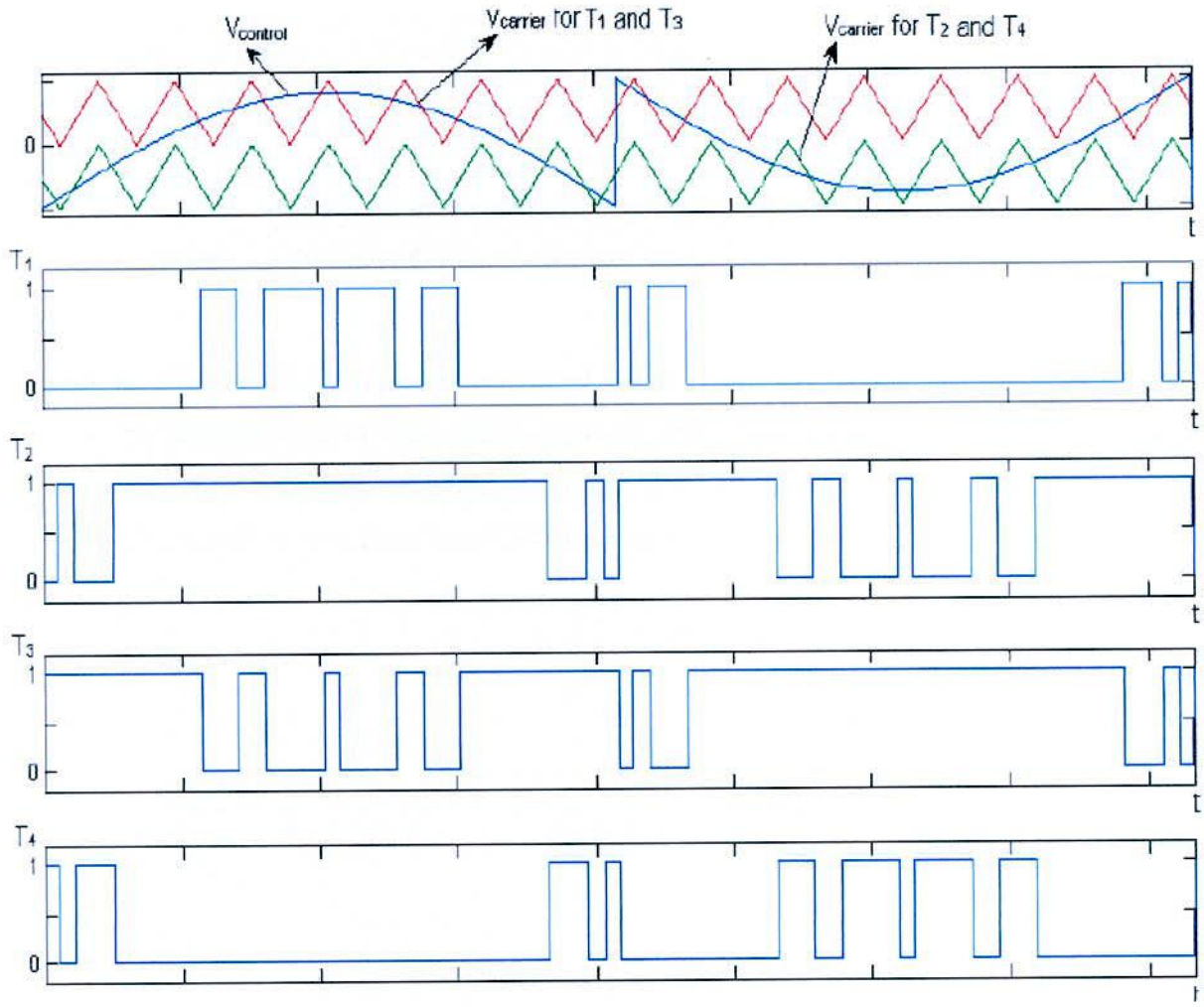


Figure 3.5 Conventional two-carrier PWM scheme and gate pulse waveforms generated

3.2.3 Improved Modulation Scheme for Asymmetric Three-Level Inverter

A more efficient SPWM approach for ATLI circuit can be developed for three-level inverter circuit. The scheme is quite different from ones above and presented in the last section. In this PWM scheme, the switching devices in two arms are driven at different frequencies. For the H-bridge arm, the two devices switch at fundamental frequency f_1 while four devices in the NPC three-level arm switch at carrier frequency fs. Figure 3.6 is an illustration of this modified PWM method. In this PWM method, for NPC three-level arm, one control signal and two carrier

signals are employed. The top triangular carrier signal is for T_1 and T_3 while the bottom triangular carrier signal is for T_2 and T_4. However, the control signal is special. Its not a regular sinusoidal signal but the sum of a sinusoidal signal and a square signal, both at the fundamental frequency as shown in Figure 3.6 (a). For H-bridge arm, the switching signal or the control signal is a simple square waveform as shown in Figure 3.6 (b). The difference between two signals for two arms makes a sinusoidal output.



(a)Gate pulse waveforms generated for NPC arm

CHAPTER 4

MICROCONTROLLER

4.1 Overview of 8051 Microcontroller

The AT89C51 (One kind of 8051 microcontroller) is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash programmable and erasable read only memory (PEROM). The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry standard MCS-51 instruction set and pin out. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly-flexible and cost-effective solution to many embedded control applications [15].

Figure 4.1 Configuration of AT89C51 Microcontroller

4.3 Pin Description

VCC

Supply voltage. +5.0V

GND

Ground.

Port 0

Port 0 is an 8-bit open-drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high impedance Inputs. Port 0 may also be configured to be the multiplexed low order address/data bus during accesses to external program and data memory. In this mode P0 has internal pull-ups. Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pull-ups are required during program verification.

Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current because of the internal pull-ups. Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2

Port 2 is an 8-bit bi-directional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current because of the internal pullups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI),

Port 2 emits the contents of the P2 Special Function Register. Port 2 also receives the high order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current because of the pull-ups.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/PROG

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming. In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALEpulse is skipped during each access to external Data Memory. If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

PSEN

Program Store Enable is the read strobe to external program memory. When the AT89C51 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

EA/VPP

External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if

lock bit 1 is programmed, EA will be internally latched on reset. EA should be strapped to VCC for internal program executions. This pin also receives the 12-volt programming enable voltage (VPP) during Flash programming, for parts that require 12-volt VPP.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

4.4 RAM Memory Space Allocation in the 8051

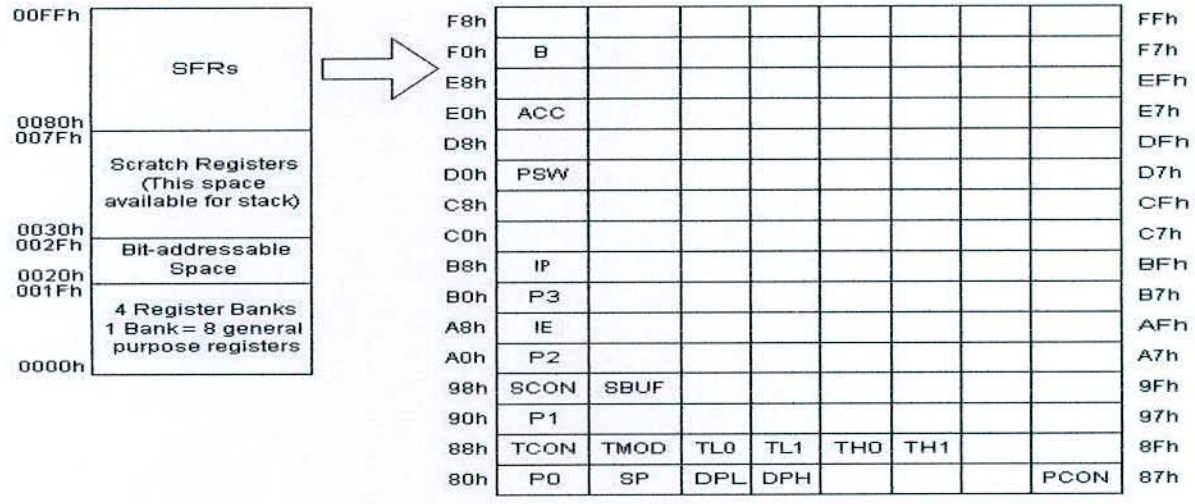


Figure 4.3 Memory space allocation of 8051

The 8051 microcontroller has a total of 128 bytes of RAM which are assigned address 00 to 7FH.These 128 bytes are divided into 3 different groups as follows.

I. A total of 32 bytes from location 00 to 1FH are set aside for register banks and the stack.

II. A total of 16 bytes from location 20H to 2FH are set aside for bit addressable read/write memory.

III. A total of 80 bytes from location 30H to 7FH are used for read and write storage, or what is normally called a "scratch pad". These 80 locations of RAM are widely used for the purpose of storing data and parameters by 8051 programmers.

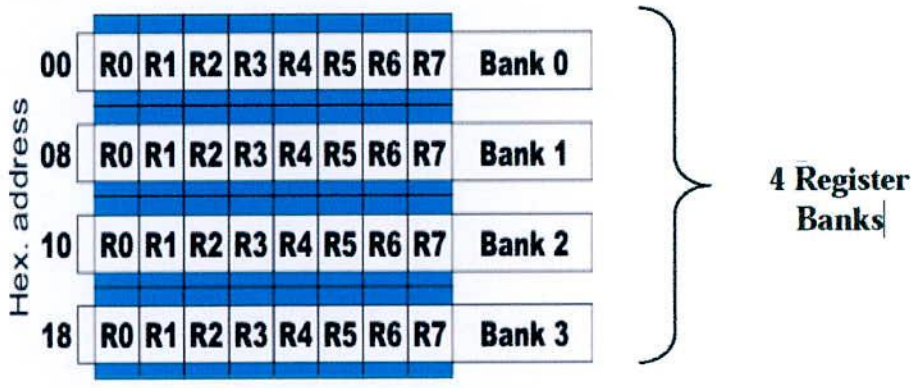


Figure 4.4 Resister bank

4.5 Basic Power Circuit of AT89C51

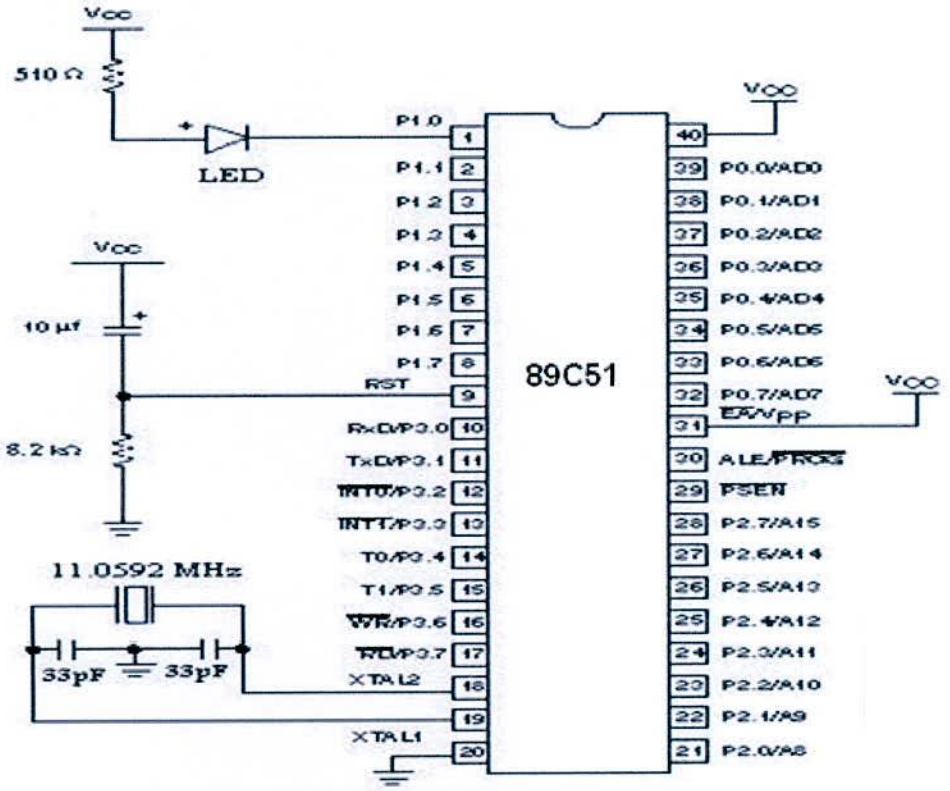


Figure 4.5 Power circuit of 8051

4.6 Assembling and Running an 8051 Program

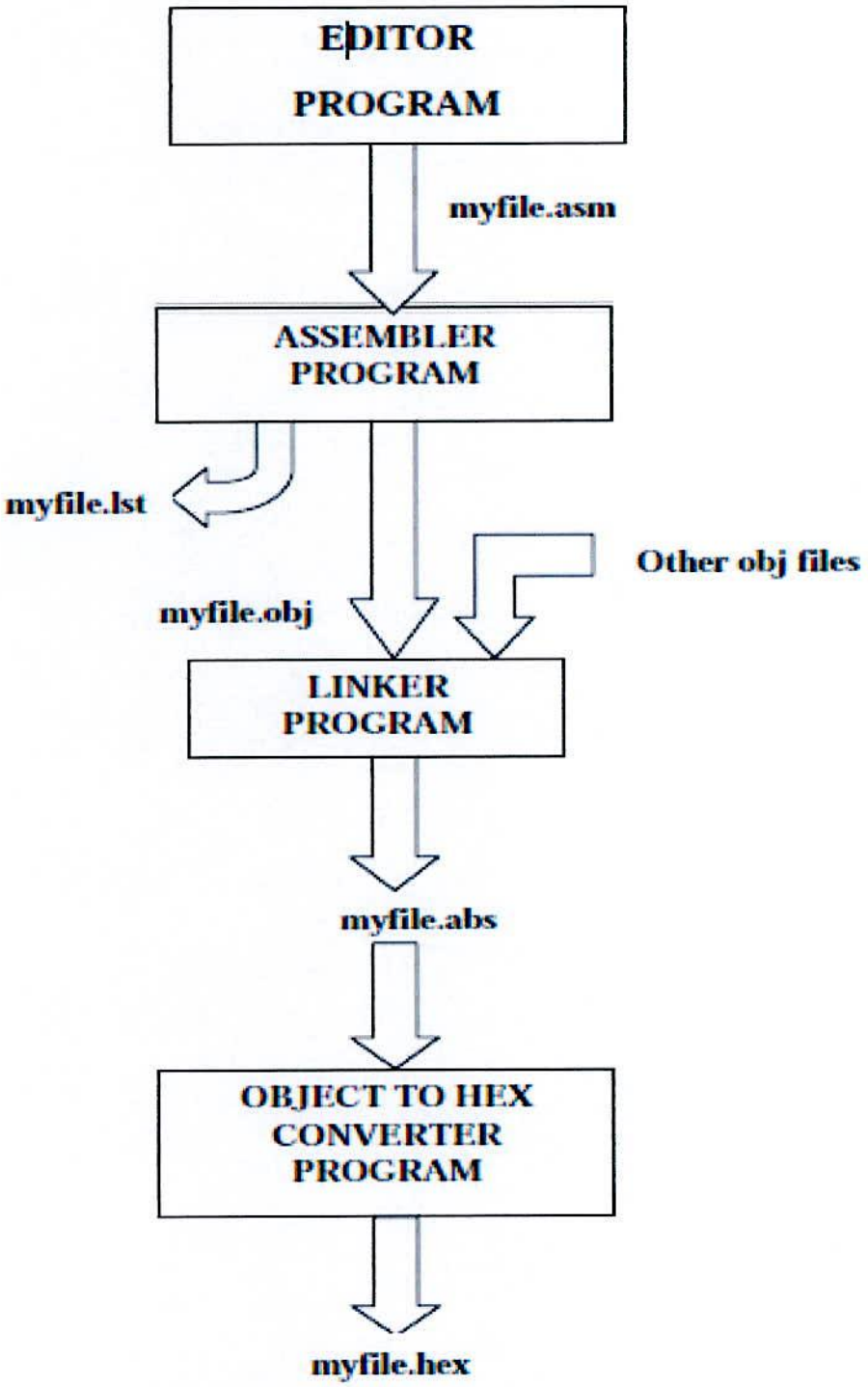


Figure 4.6 Flow chart of microcontroller programming

CHAPTER 5

GATE PULSE GENERATION USING MICROCONTROLLER

5.1 Different technique

There are two ways for generating gate pulse by using microcontroller :

i) Indirect generation

ii) Direct generation

Indirect technique is more complicated and costly than direct technique and some time it doesn't give the desired output. In Indirect technique all the component need to be synchronized at a time.

5.2 Indirect technique

In this technique at first the desired analog sine wave , analog triangular wave is generated by using digital to analog converter (DAC) and then compare by a comparator. By comparing two signal the gate pulse will be generated.

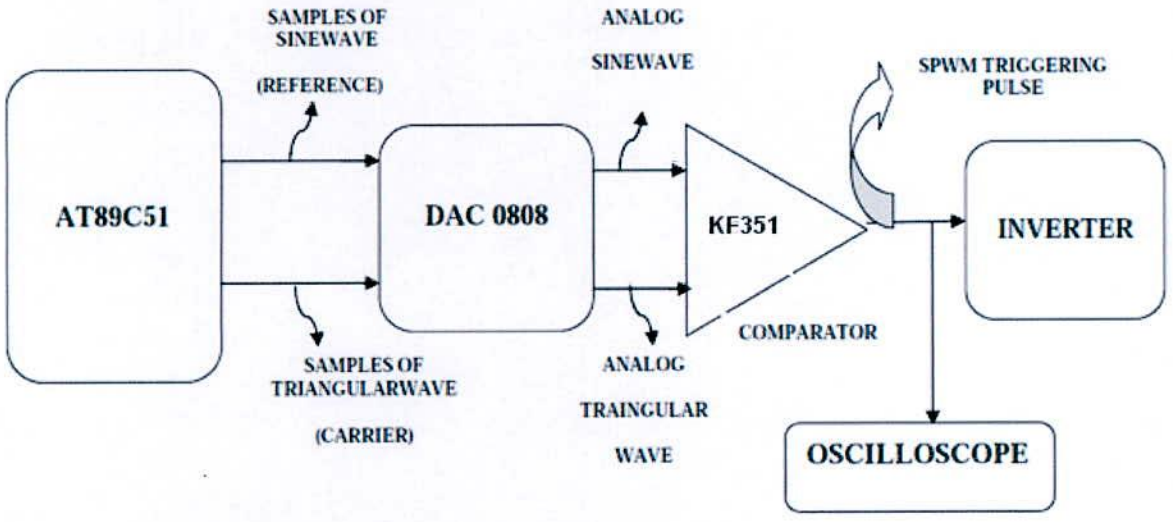


Figure 5.1 Block diagram representation of Indirect technique

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5.2.1 Algorithm for PWM Wave Generation:

I. Compilation and Simulation of Assembly language program for AT89C51 using "Top view simulator(4.1)"

II. Burning the Program through the "BeeProg universal(48pin Driver) Programmer" into the flash memory of AT89C51

III. Generation of Digital Sample of Sinusoidal and Triangular waves from microcontroller, which is fed into the DAC 0808

IV. Analog output from the DAC 0808 is fed into the comparator KF351

V. Generation of SPWM triggering pulses from KF351 (which is observed through the Oscilloscope) fed to the inverter

5.2.2 Interfacing AT89C51 With DAC 0808

The Digital to Analog converter is a device widely used to convert digital pulses to analog signal. There are two methods of making the DAC namely, Binary weighted and R/2R ladder. The vast majority of integrated circuit DACs, use the R/2R method. Since, it can achieve much higher degree of precision. The first criterion for judging a DAC is its resolution, which is a function of the number of binary inputs. The common ones are 8,10 and 12 bits. The number of data bit inputs decides the resolution of the DAC since the number of analog output levels is equal to 2^n ,where n is the number of data bit inputs. There are also 16 bit DACs but they are expensive. The DAC 0808 is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (IREF) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 IREF/256. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range. In DAC 0808 the digital inputs are converted to current (Iout) and by connecting a resistor to the Iout pin we convert the result to voltage. The total current provided by the Iout pin is a function of the binary number at D0-D7 inputs of the DAC 0808 and the reference current Iref is

as follows.

$I_{out} = I_{ref}$ (D7/2 +D6/4 + D5/8 + D4/16 + D3/32 + D2/64 + D1/128 + D0/256)

Where D0 is the LSB and D7 is the MSB for the inputs and Iref is the input current that must be applied to pin 14.The output pin Iout is connected to resistor and converts this current to voltage and the output can be monitored on the scope.

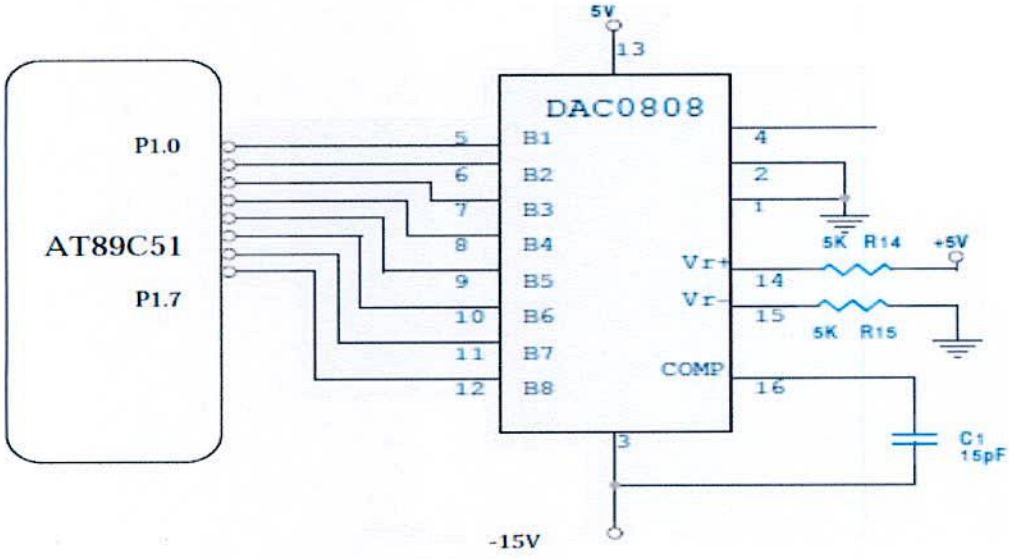

Figure 5.2 Circuit diagram showing interfacing AT89C51 with DAC 0808

5.2.3 Features

- Relative accuracy: ±0.19% error maximum
- Full scale current match: ±1 LSB type
- Fast settling time: 150 ns type
- Non inverting digital inputs are TTL and CMOS
- compatible
- High speed multiplying input slew rate: 8 mA/μs
- Power supply voltage range: ±4.5V to ±18V
- Low power consumption: 33 mW @ ±5V

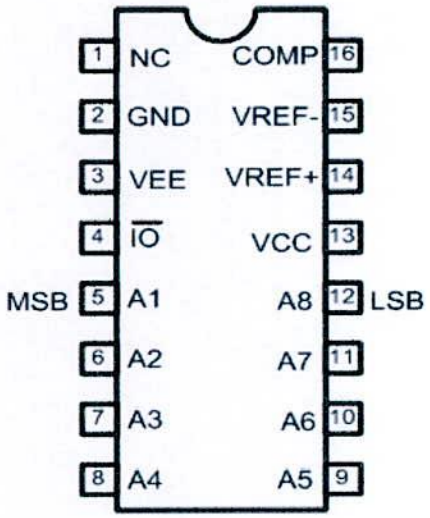

Figure 5.3 Pin Description of DAC 0808

5.2.4 Interfacing DAC0808 With KF351 Comparator

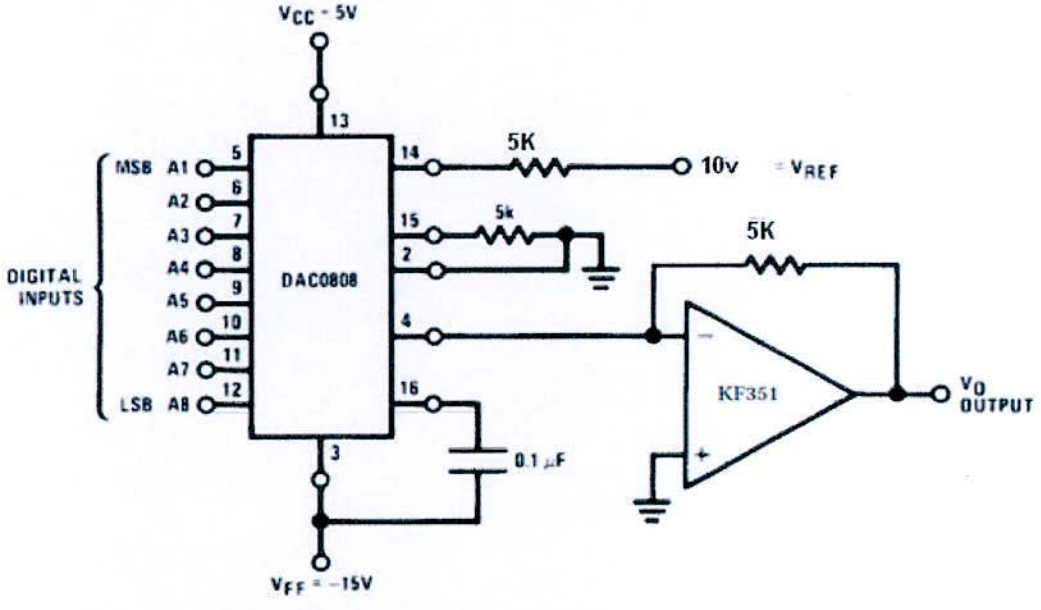

Figure 5.4 Circuit diagram showing interfacing DAC0808 with KF351

In this technique microcontroller processing a list of digital data. From this data analog signal is generated by using digital to analog converter (DAC).This analog signal than compare with each other and gives the desired modulation technique. In this technique DAC and comparator is need that makes inverter costly and complicated than direct technique.

5.3 Direct generation

In direct technique it is not necessary to think about the carrier signal and control signal like the modulation technique. In this process the gate pulse are generated from microcontroller by giving the output port high(1) and low(0) and control the frequency by changing the delay time in between two pulse.Assume a modulation technique (modified PWM taken because it gives better performance than others) as shown in Fig 5.5 and Fig 5.6.

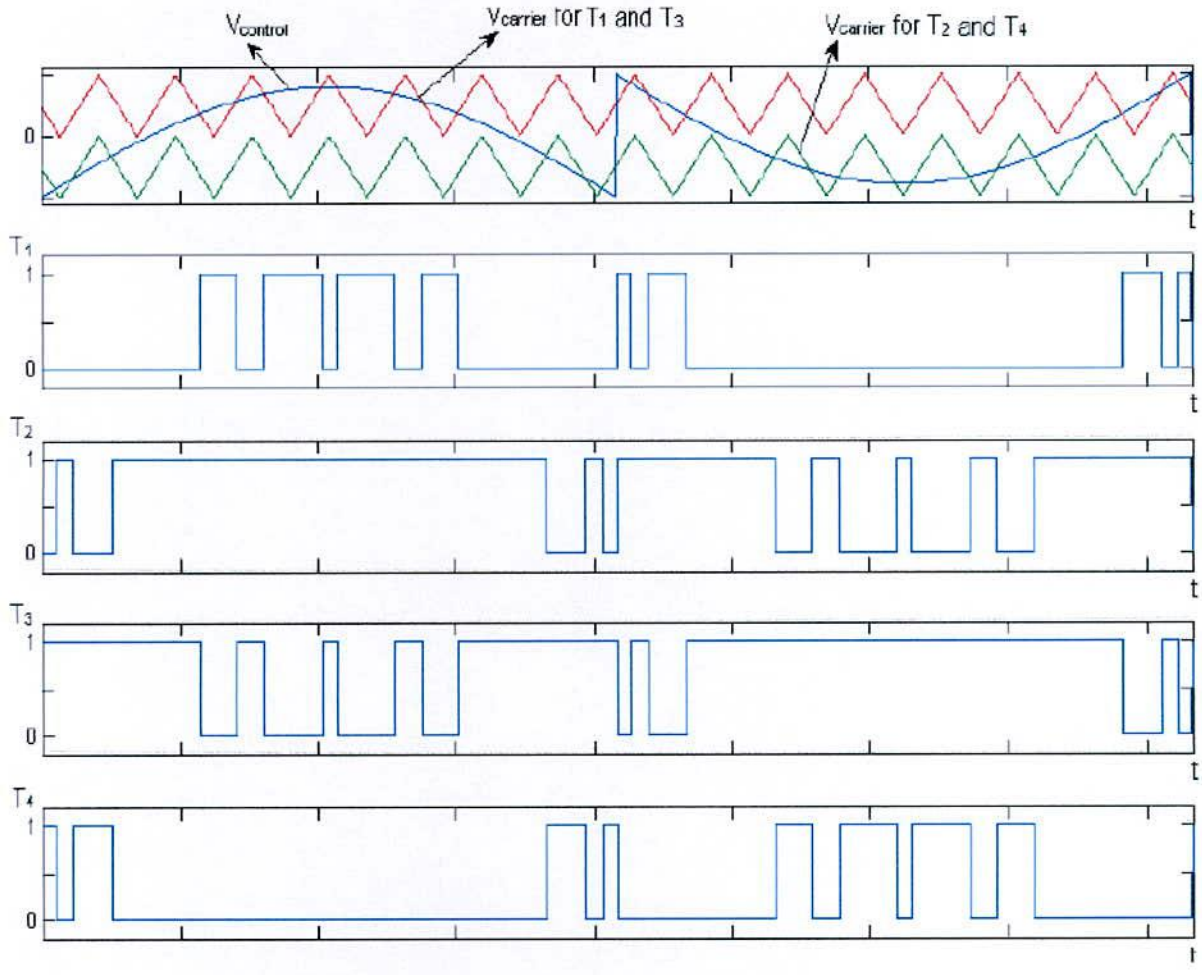

Figure 5.5 Gate pulse waveforms generated for NPC arm

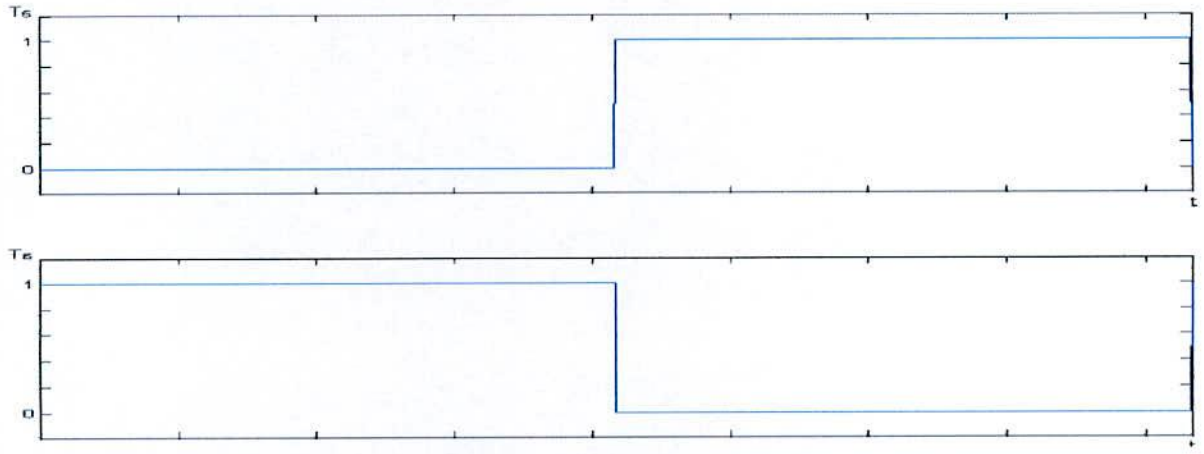

Figure 5.6 Gate pulse waveforms generated for H-bridge arm

Now it is wanted to generate gate pulse for T_1 as shown in figure 4.6 ,than we give the high and low bit of the output port continuously. But in this diagram the high bit width and low bit width is not same. For that reason at first the total time is divided into small unit that is equal to the small pulse width and then give high bit and low bit to generate gate pulse of T_1 as shown in below.

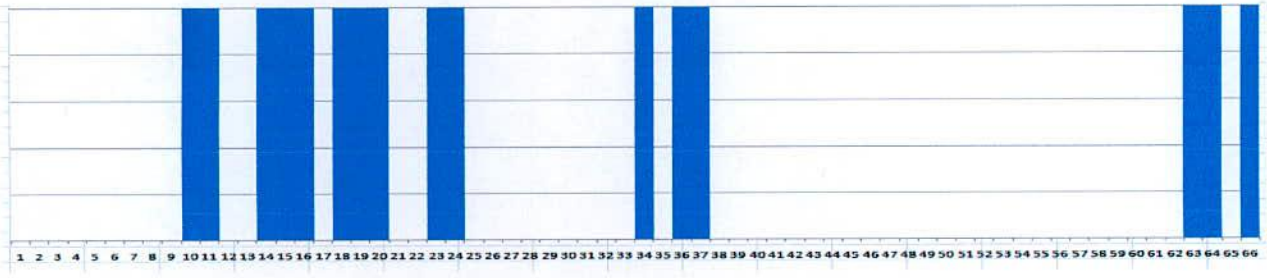

Figure 5.7 Gate pulse generation for T_1 by using microcontroller

Similarly we can easily generate T_2,T_3,T_4,T_5,T_6 as shown in figure below.

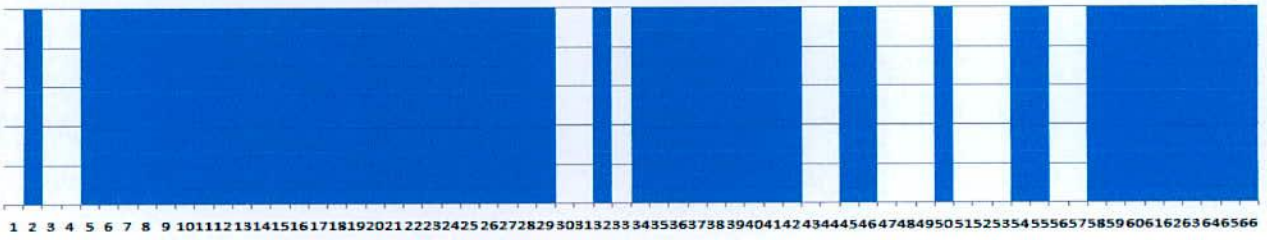

Figure 5.8 Gate pulse generation for T_2 by using microcontroller

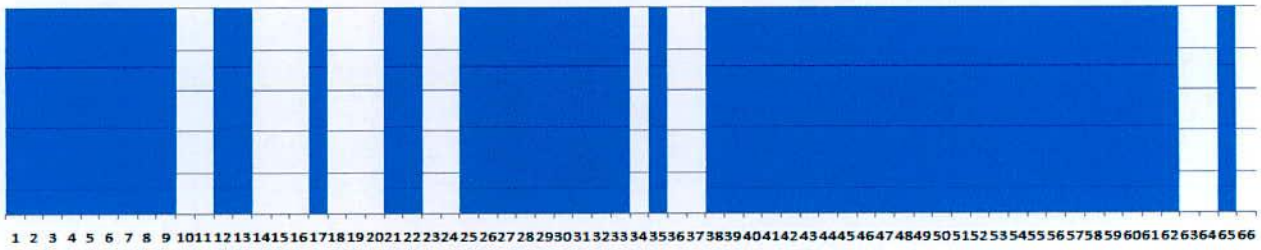

Figure 5.9 Gate pulse generation for T_3 by using microcontroller

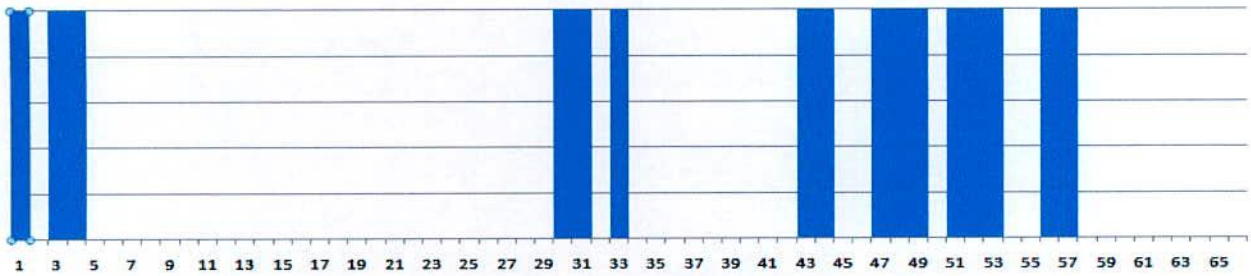

Figure 5.10 Gate pulse generation for T_4 by using microcontroller

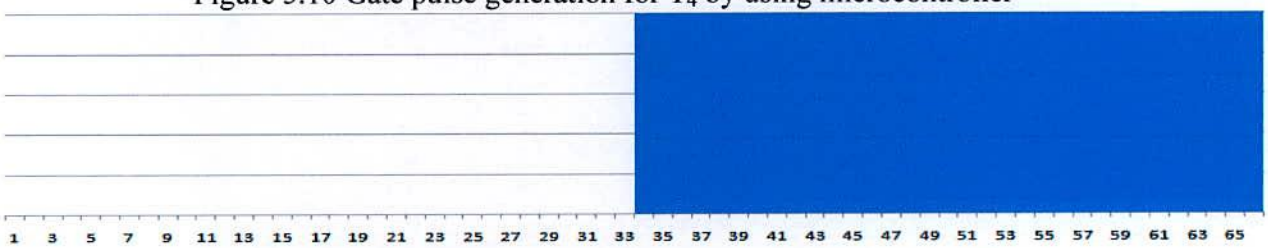

Figure 5.11 Gate pulse generation for T_5 by using microcontroller

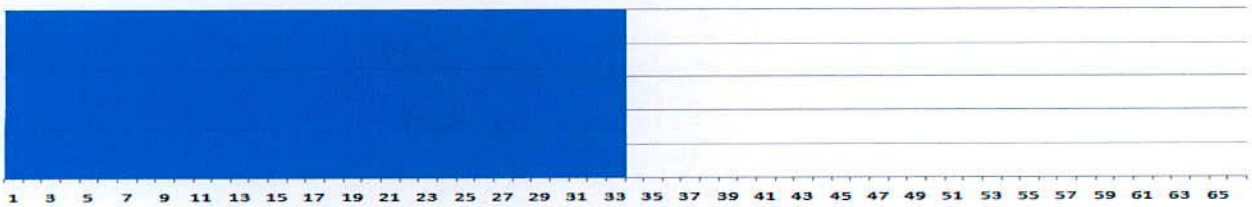

Figure 5.12 Gate pulse generation for $\bar{T}_6$ by using microcontroller

From this switching pattern now we can easily made a table of switching states as shown figure below. From this table we also easily made microcontroller Assembly program (see Appendix A) which generate the desired output gate pulse for IGBT. This process is so much easy, less complexity and lower cost method . So that in this project this process is followed.

Table 5.1 Switching States of Gate pulse for ALTI (modified PWM)

	T1	T2	T3	T4	T5	T6
1	0	0	1	1	0	1
2	0	1	1	0	0	1
3	0	0	1	1	0	1
4	0	0	1	1	0	1
5	0	1	1	0	0	1
6	0	1	1	0	0	1
7	0	1	1	0	0	1
8	0	1	1	0	0	1
9	0	1	1	0	0	1
10	1	1	0	0	0	1
11	1	1	0	0	0	1
12	0	1	1	0	0	1
13	0	1	1	0	0	1
14	1	1	0	0	0	1
15	1	1	0	0	0	1
16	1	1	0	0	0	1
17	0	1	1	0	0	1
18	1	1	0	0	0	1
19	1	1	0	0	0	1
20	1	1	0	0	0	1
21	0	1	1	0	0	1
22	0	1	1	0	0	1
23	1	1	0	0	0	1
24	1	1	0	0	0	1
25	0	1	1	0	0	1
26	0	1	1	0	0	1
27	0	1	1	0	0	1
28	0	1	1	0	0	1
29	0	1	1	0	0	1
30	0	0	1	1	0	1
31	0	0	1	1	0	1
32	0	1	1	0	0	1
33	0	0	1	1	0	1
34	1	1	0	0	1	0
35	0	1	1	0	1	0

	T1	T2	T3	T4	T5	T6
36	1	1	0	0	1	0
37	1	1	0	0	1	0
38	0	1	1	0	1	0
39	0	1	1	0	1	0
40	0	1	1	0	1	0
41	0	1	1	0	1	0
42	0	1	1	0	1	0
43	0	0	1	1	1	0
44	0	0	1	1	1	0
45	0	1	1	0	1	0
46	0	1	1	0	1	0
47	0	0	1	1	1	0
48	0	0	1	1	1	0
49	0	0	1	1	1	0
50	0	1	1	0	1	0
51	0	0	1	1	1	0
52	0	0	1	1	1	0
53	0	0	1	1	1	0
54	0	1	1	0	1	0
55	0	1	1	0	1	0
56	0	0	1	1	1	0
57	0	0	1	1	1	0
58	0	1	1	0	1	0
59	0	1	1	0	1	0
60	0	1	1	0	1	0
61	0	1	1	0	1	0
62	0	1	1	0	1	0
63	1	1	0	0	1	0
64	1	1	0	0	1	0
65	0	1	1	0	1	0
66	1	1	0	0	1	0

CHAPTER 6

MICROCONTROLLER BASED IMPLEMENTATION

6.1 Practical Implementation

A circuit interface for the experimental system of ATLI is given in Figure 6.2. The diagram illustrates the main power circuit, microcontroller, output filter, and the load with detailed interfacing signals. A hardware prototype of asymmetric three-level inverter as shown in Figure 3.3 and Figure 6.2 is used in this experiment. It's a part of a three-phase inverter designed and built by Dr. J. Chang [4]. Only two arms of this three-phase inverter are used to make a single-phase asymmetric three-level inverter. Figure 6.1 below is a pictorial view of the practical prototype.

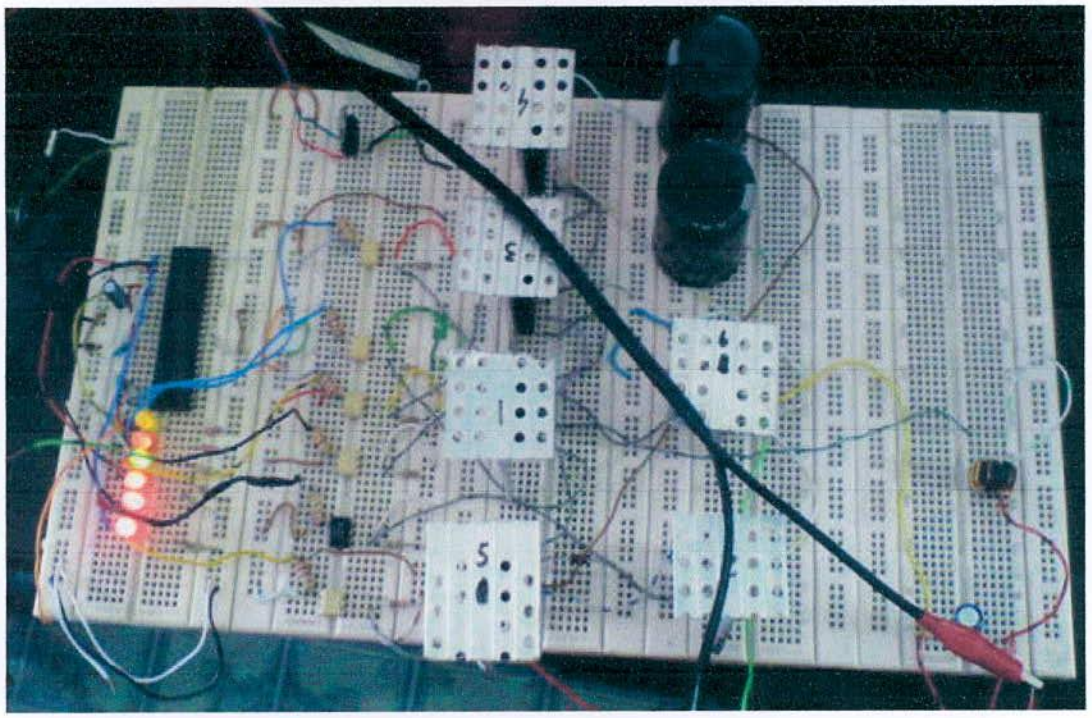

Figure 6.1 A picture of ATLI prototype

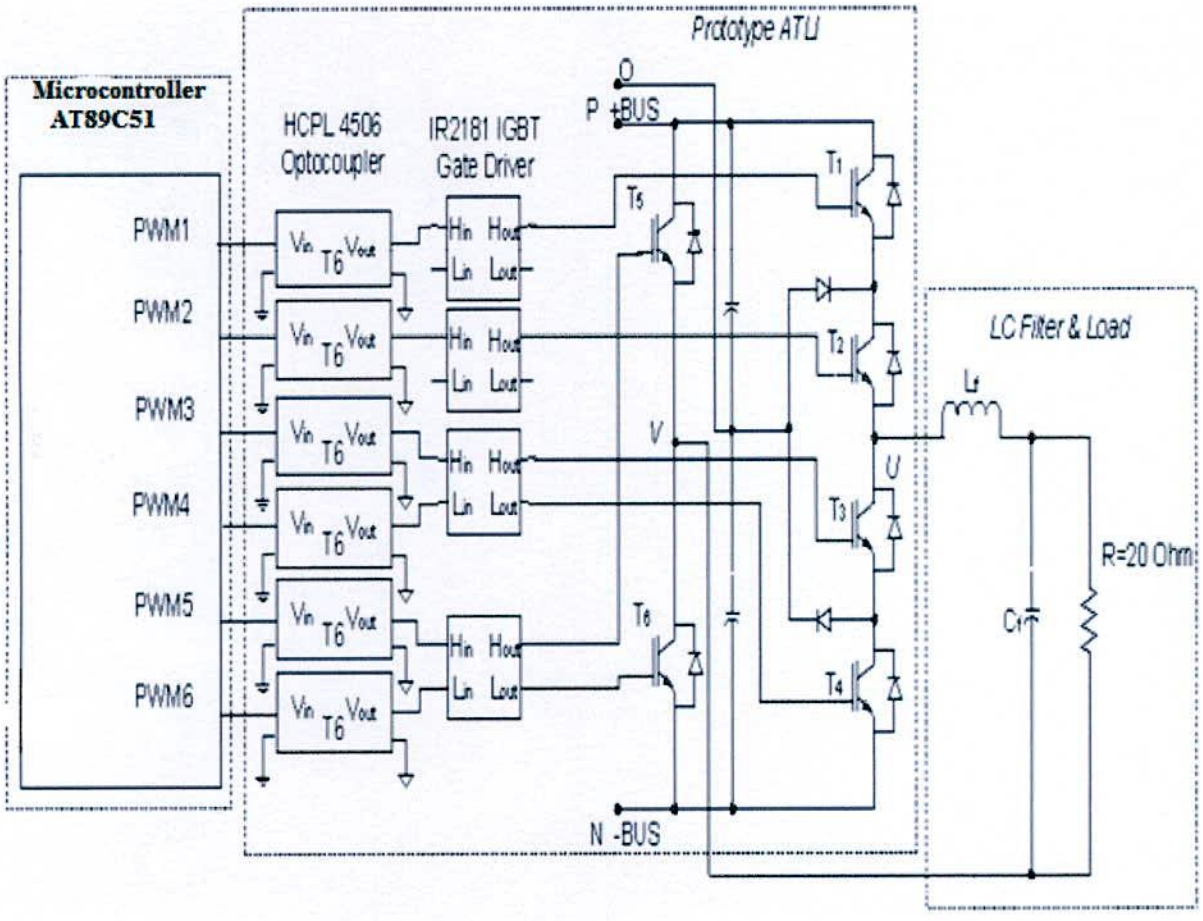

Figure 6.2 Circuit interface for the experimental system

The prototype of ATLI can be divided into two sections:

1. The main circuit board. The IGBT modules FII 30-06D with fast and soft recovery diode are used as the switching devices in ATLI. The voltage rating of this IGBT is 600V.

2. The power interfacing board. The decoupling and driving circuits are on this power interfacing board. In the decoupling circuit, the HCPL-4506 Optocoupler modules are used for isolating between microcontroller output signal and the converter high voltage circuits. In the driving circuit, four IR2181s the high voltage, high speed MOSFET/IGBT gate driver chip are used to drive the IGBT devices in converter. An IR2181 can drive two IGBTs (high side and low side) simultaneously. However, due to the special configuration of ATLI, three IR2181 chips instead

of two are needed to drive the IGBTs in NPC arm. For the IGBT T1 and T3 in Figure 3.3, only high side outputs of two IR2181 are used for decoupling reason. Figure 6.2 shows the interconnections of the optocouplers and gate drivers.

6.2 LC filter and Load

The output voltage frequency in this experiment is 50 Hz. For this frequency we need a second order LC filter to remove the noise and harmonics. The configurations of the second order LC filter and load are shown in Figure 6.3.

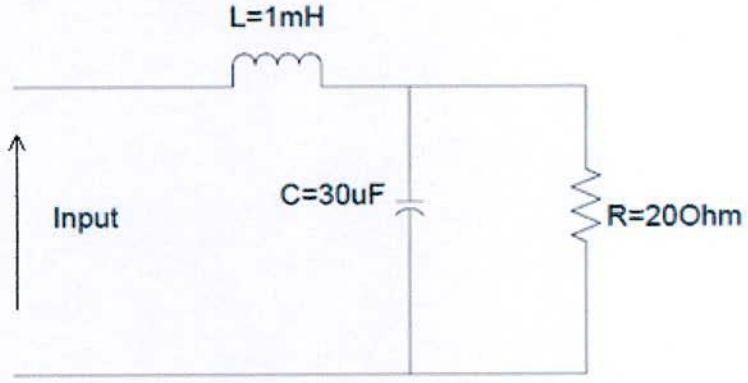

Figure 6.3 LC filter & load configuration

6.3 Experimental System Setup

Figure 6.4 shows an overview of the lab experiment prototype system.

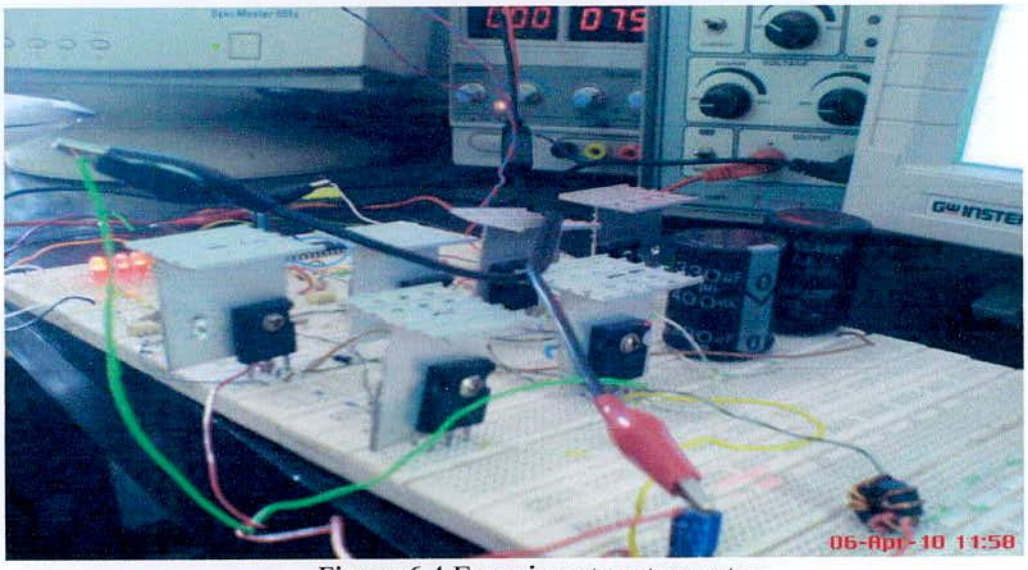

Figure 6.4 Experiment system setup.

6.4 Circuit Interface

The configurations of components in the experimental system are discussed in section 6.1. In this section, the interface between these components will be described. Figure 6.2 shows the general interface configuration between different components. The gate pulse output pins from microcontroller provide the input to the decoupling circuit. The outputs of the optocouplers are connected to the corresponding IGBT drivers; the output of these gate drivers are connected to the gate drive input ports of IGBTs in the ATLI power circuit. Finally power output of the two phase circuit, the U and V phase of the ATLI are connected to a LC filter followed by a resistance load, as shown in figure 6.2.

6.5 Experimental Results

The gate pulse of microcontroller for ALTI is shown below.

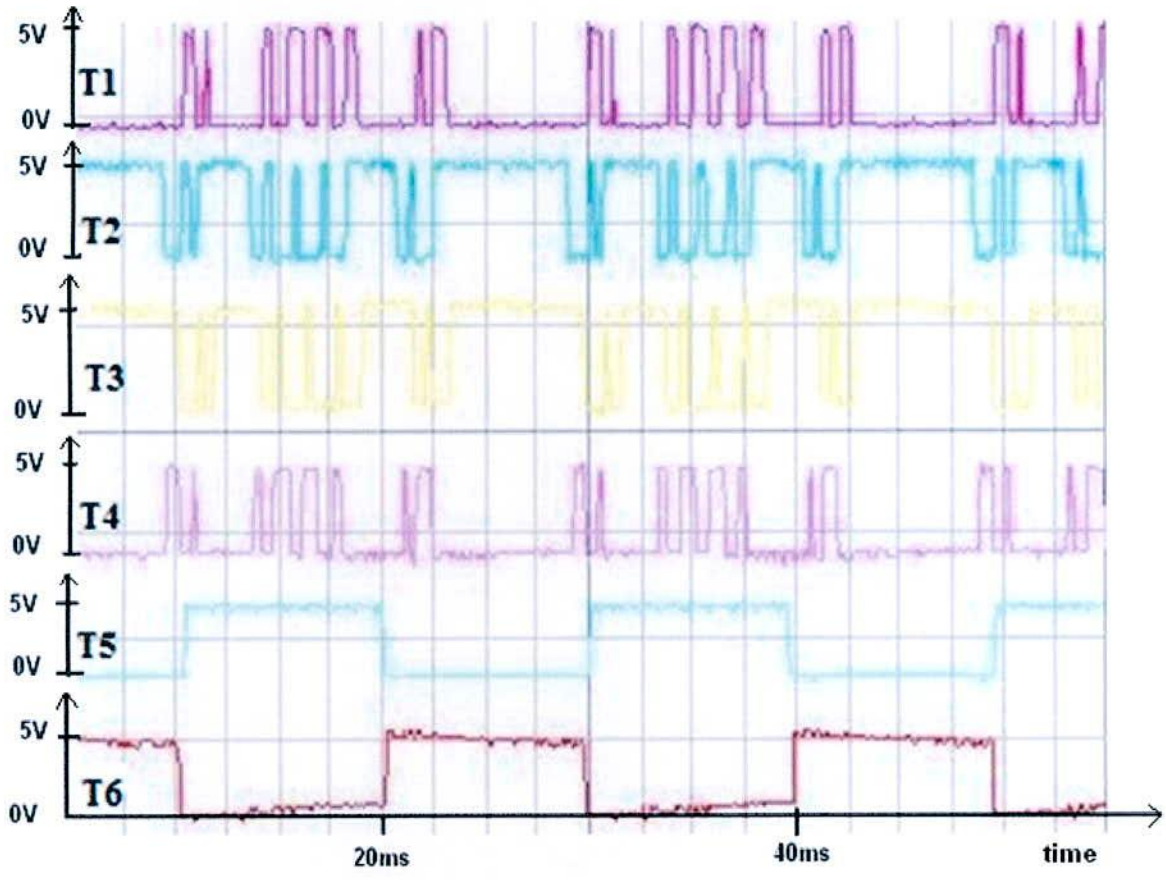

Figure 6.5 Generated Gate pulse for IGBT using microcontroller

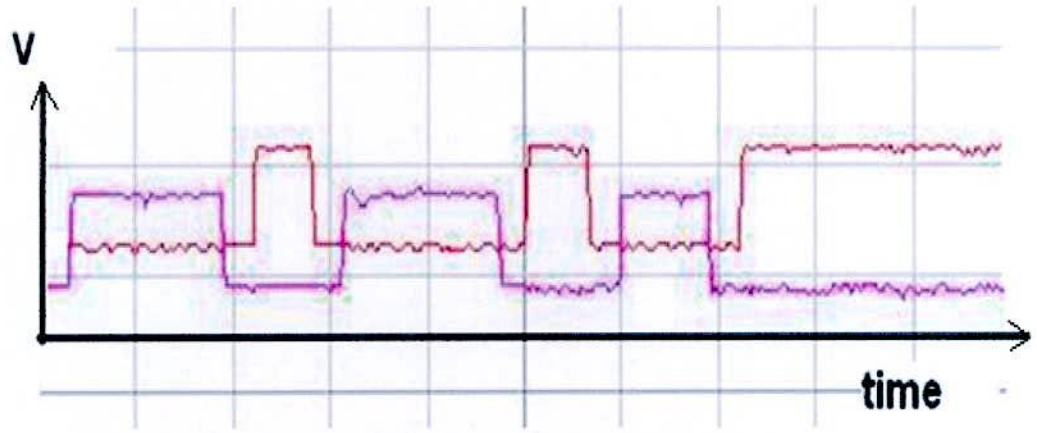

Figure 6.6 Dead band time generation between T_1 and T_3 using microcontroller

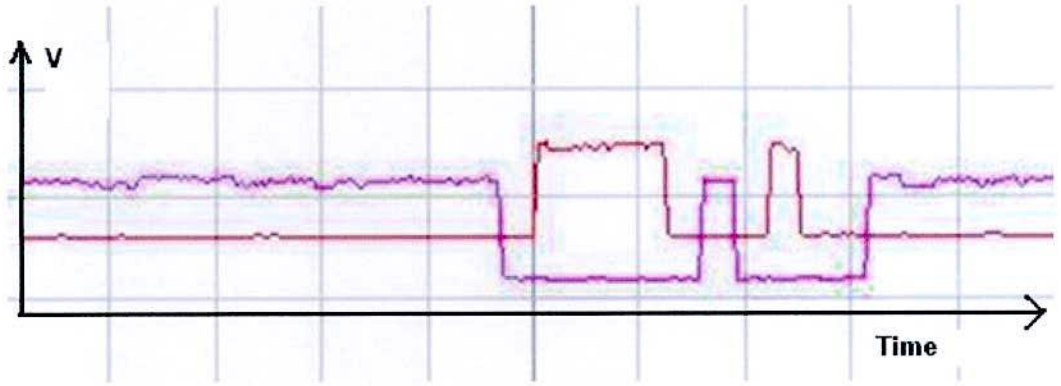

Figure 6.7 Dead band time generation between T_2 and T_4 using microcontroller

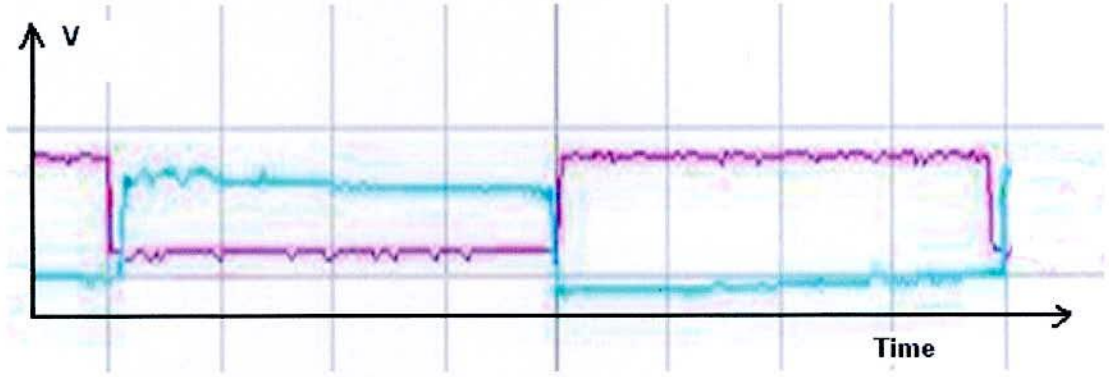

Figure 6.8 Dead band time generation between T_5 and T_5 using microcontroller

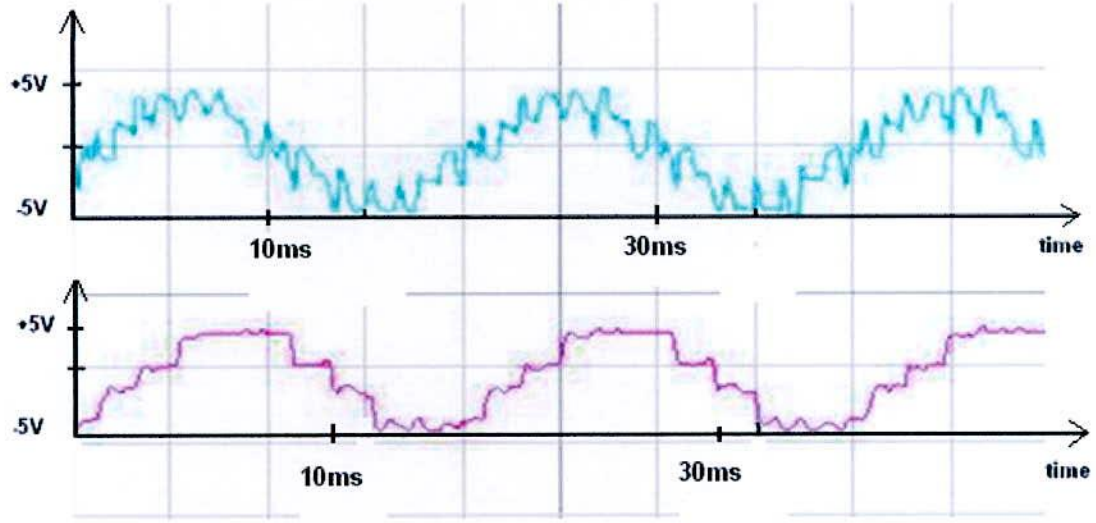

Figure 6.9 Output voltage waveforms before and after LC filter at 50 Hz

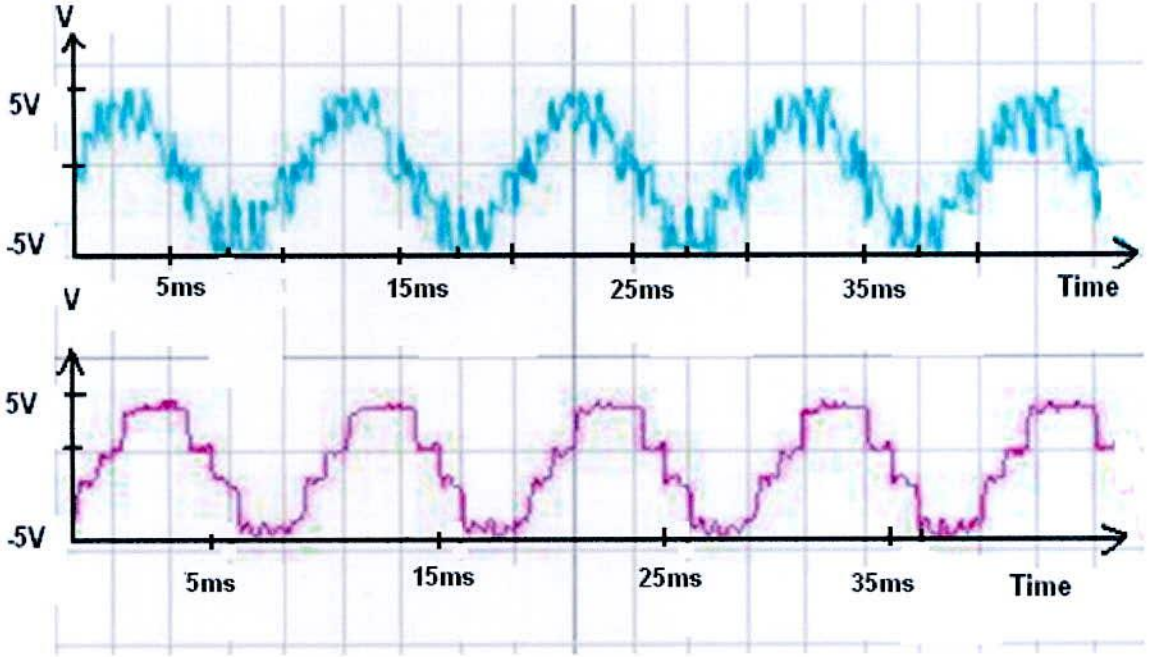

Figure 6.10 Output voltage waveforms before and after LC filter at 100 Hz

CHAPTER 7

CONCLUSIONS

7.1 Conclusion

In this project a latest topology of single-phase DC-AC inverter-asymmetric three-level inverter (ATLI) is implemented and a microcontroller control scheme is discussed. The discussion of ATLI and microcontroller control scheme is detailed using the following approaches: 1) Theoretical analysis of the advantages of the ATLI power circuit topology over other topologies. 2) Theoretical analysis of microcontroller control scheme. 3) Hardware implementation of the core converter circuit based on microcontroller. The asymmetric three-level inverter with microcontroller control scheme surpasses conventional H-bridge converter and NPC converter in lower harmonic distortion (THD), reduction of high-frequency EMI noise, lower power loss and increased performance-to-cost ratio. Hardware implementation and experimental results are given in chapter 6, which verifies the feasibility of ATLI and microcontroller control scheme. The AT89C51 microcontroller used satisfies the control requirement of the high switching frequency schemes.

7.2 Future Research Works

In this project, an open-loop asymmetric three-level inverter is developed and discussed. There are several aspects that can be improved in the future:

1. In recent years, many multi-level inverter topologies are proposed and analyzed in order to further reduce harmonic components of the output voltage and current [16-17]. These topologies have more voltage levels and are derivations from the three-level topology by adding more switching devices to the bridge circuit. Therefore, the complexity of circuit topology and microcontroller control scheme for the multilevel topology will be increased. More efforts are needed to explore advanced solutions balanced between better performance and lower control complexity as well as cost.

2. In many applications such as AC motor drive, adjustable frequency, amplitude and phase of output voltage from inverter are required; therefore, a close-loop controller is necessary for the inverter. Many novel control methods are developed in recent years, like sliding mode control, back stepping motion control [18-19]; Applying these control method in ATLI conversion system will be an interesting research topic in the future.

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Appendix A

MICROCONTROLLER PROGRAMMING FOR GATE PULSE WAVEFORM GENERATION

```
#include <REGX51.H>
#include <intrins.h>
sbit PWM1 = P1^0;
sbit PWM2 = P1^1;
sbit PWM3 = P1^2;
sbit PWM4 = P1^3;
sbit PWM5 = P1^4;
sbit PWM6 = P1^5;

void MSDelay(int i)
{
 while(--i)
 {
  _nop_();
  _nop_();
  _nop_();
  _nop_();
 }
}
void main(void)
{
        while(1)
  {

   PWM1 = 0;   //1
   PWM2 = 0;
   PWM3 = 1;
   PWM4 = 1;
   PWM5 = 0;
   PWM6 = 1;
   MSDelay(35);

   PWM1 = 0;   //2
   PWM2 = 1;
   PWM3 = 1;
   PWM4 = 0;
   PWM5 = 0;
   PWM6 = 1;
   MSDelay(35);

   PWM1 = 0;   //3
   PWM2 = 0;
   PWM3 = 1;
   PWM4 = 1;
   PWM5 = 0;
   PWM6 = 1;
   MSDelay(35);

   PWM1 = 0;   //4
   PWM2 = 0;
   PWM3 = 1;
   PWM4 = 1;
   PWM5 = 0;
```

```
PWM6 = 1;
MSDelay(35);

PWM1 = 0;  //5
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 0;  //6
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 0;  //7
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 0;  //8
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 0;  //9
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 1;  //10
PWM2 = 1;
PWM3 = 0;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 1;  //11
PWM2 = 1;
PWM3 = 0;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 0;  //12
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
```

```
MSDelay(35);

PWM1 = 0;  //13
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 1;  //14
PWM2 = 1;
PWM3 = 0;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 1;  //15
PWM2 = 1;
PWM3 = 0;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 1;  //16
PWM2 = 1;
PWM3 = 0;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 0;  //17
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 1;  //18
PWM2 = 1;
PWM3 = 0;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 1;  //19
PWM2 = 1;
PWM3 = 0;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 1;  //20
PWM2 = 1;
PWM3 = 0;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
```

```
MSDelay(35);

PWM1 = 0;  //21
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 0;  //22
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 1;  //23
PWM2 = 1;
PWM3 = 0;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 1;  //24
PWM2 = 1;
PWM3 = 0;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 0;  //25
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 0;  //26
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 0;  //27
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 0;  //28
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
```

```
MSDelay(35);

PWM1 = 0;  //29
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 0;  //30
PWM2 = 0;
PWM3 = 1;
PWM4 = 1;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 0;  //31
PWM2 = 0;
PWM3 = 1;
PWM4 = 1;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 0;  //32
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 0;  //33
PWM2 = 0;
PWM3 = 1;
PWM4 = 1;
PWM5 = 0;
PWM6 = 1;
MSDelay(35);

PWM1 = 1;  //34
PWM2 = 1;
PWM3 = 0;
PWM4 = 0;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 0;  //35
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 1;  //36
PWM2 = 1;
PWM3 = 0;
PWM4 = 0;
PWM5 = 1;
PWM6 = 0;
```

```
MSDelay(35);

PWM1 = 1;  //37
PWM2 = 1;
PWM3 = 0;
PWM4 = 0;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 0;  //38
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 0;  //39
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 0;  //40
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 0;  //41
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 0;  //42
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 0;  //43
PWM2 = 0;
PWM3 = 1;
PWM4 = 1;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 0;  //44
PWM2 = 0;
PWM3 = 1;
PWM4 = 1;
PWM5 = 1;
PWM6 = 0;
```

```
MSDelay(35);

PWM1 = 0;  //45
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 0;  //46
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 0;  //47
PWM2 = 0;
PWM3 = 1;
PWM4 = 1;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 0;  //48
PWM2 = 0;
PWM3 = 1;
PWM4 = 1;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 0;  //49
PWM2 = 0;
PWM3 = 1;
PWM4 = 1;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 0;  //50
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 0;  //51
PWM2 = 0;
PWM3 = 1;
PWM4 = 1;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 0;  //52
PWM2 = 0;
PWM3 = 1;
PWM4 = 1;
PWM5 = 1;
PWM6 = 0;
```

```
MSDelay(35);

PWM1 = 0;  //53
PWM2 = 0;
PWM3 = 1;
PWM4 = 1;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 0;  //54
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 0;  //55
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 0;  //56
PWM2 = 0;
PWM3 = 1;
PWM4 = 1;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 0;  //57
PWM2 = 0;
PWM3 = 1;
PWM4 = 1;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 0;  //58
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 0;  //59
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 0;  //60
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 1;
PWM6 = 0;
```

```
MSDelay(35);

PWM1 = 0;  //61
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 0;  //62
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 1;  //63
PWM2 = 1;
PWM3 = 0;
PWM4 = 0;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 1;  //64
PWM2 = 1;
PWM3 = 0;
PWM4 = 0;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 0;  //65
PWM2 = 1;
PWM3 = 1;
PWM4 = 0;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);

PWM1 = 1;  //66
PWM2 = 1;
PWM3 = 0;
PWM4 = 0;
PWM5 = 1;
PWM6 = 0;
MSDelay(35);
  }
}
```