Capacitance-Voltage Characterization of Ultra Scaled XOI FET: An Analytical Approach

By

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A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Engineering in the Department of Electrical and Electronic Engineering

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Declaration

This is to certify that the thesis work entitled "**Capacitance-Voltage Characterization of Ultra Scaled XOI FET: An Analytical Approach**" has been carried out by **Muhammad Mainul Islam** in the Department of **Electrical and Electronic Engineering**, Khulna University of Engineering & Technology, Khulna, Bangladesh. The above thesis work or any part of this work has not been submitted anywhere for the award of any degree or diploma.

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This is to certify that the thesis work submitted by **Muhammad Mainul Islam** entitled "**Capacitance-Voltage Characterization of Ultra Scaled XOI FET: An Analytical Approach**" has been approved by the board of examiners for the partial fulfillment of the requirements for the degree of **M.Sc. Engineering** in the Department of **Electrical and Electronic Engineering**, Khulna University of Engineering & Technology, Khulna, Bangladesh in July 2017.

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*A*bstract

Device scaling is the key factor that drives the microelectronics revolution as described by Moore's law. Reduction of the physical MOS device dimensions has been proved beneficial in terms of circuit speed, cost and power consumption. But the continued miniaturization of the MOS transistor imposes a lot of challenges in terms of device design. Addressing to this issue "Compound semiconductor-on-insulator" was reported in 2010, which is also termed as XOI**.** III-V materials can be considered as the perfect replacement of silicon as the channel material in MOS devices due to their excellent transport properties. It is well established that the capacitance – voltage (C-V) measurement is widely accepted technique for different device parameter extraction and also to measure the interface quality of a fabricated MOSFET. An analytical model is developed here using quantum mechanical approach to explain the C-V characteristics of XOI FET by solving coupled Schrodinger-Poisson equation. It is found that the energy quantization effect in such short channel device causes a unique staircase nature in the C-V characteristics for channel thickness up to 20nm. Beyond that this nature disappear reproducing traditional C-V characteristics of SOI FET. It is also seen that channel thickness and dopant impurity has an impact on the shift of C-V curve. The threshold voltage of such devices is found higher at reduced channel thickness.

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ABBREVIATIONS

ITRS	International Technology Roadmap for Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect-Transistor
UTB	Ultra-thin-body
SOI	Silicon on Insulator
XOI	Anything on Insulator in general. In this thesis, III-V on insulator
EOT	Equivalent Oxide Thickness
DGMOS	Double Gate MOS
CNL	Charge Neutrality Level
SCE	Short Channel Effect
PD	Partially Depleted
FD	Fully Depleted
SS	Subthreshold Slope
DIBL	Drain Induced Barrier Lowering
ALD	Atomic Layer Deposition
CBM	Conduction Band Minima
VBM	Valence Band Maxima

Chapter 1

Introduction

Chapter Outlines

- Introduction
- Scaling Issues
- Overcoming scaling issues
- Thesis objectives
- Thesis layouts

1.1 INTRODUCTION

Silicon CMOS technology has been the predominating technology in the microelectronics industry over the last few decades [1]. The advancement of CMOS technology is governed by the Moore's law, which states that the number of transistors in a dense integrated circuit has doubled approximately in every two years [2]. The continuous miniaturization of CMOS technology has enabled integrated circuit with higher packing density, performances improvement, faster circuit speed and lower power consumption [3]-[5].These key features have made their application in communication, memory chips and in microprocessor [6]-[8]. But the scaling down phenomenon arises some barriers in device design which hinders the future application of CMOS technology.

1.2 Scaling Issues

1.2.1: Processor power

Processor power is one of the key issues in modern chip design. The increased number of transistor per chip causes the processor power to be increased due to increased die size and fast frequency scaling [9]. But the die and frequency scaling were stopped when the power dissipation reached to 100W per chip. So a power constrained was set to limit the power dissipation in devices [10]. To improve the packing density of transistor, the supply voltage needed to be scaled. For optimized device performance, scaling of threshold voltage is necessary with the scaling of supply voltage as subthreshold leakage depends on threshold voltage. Scaling of supply voltage without scaling the threshold voltage would lead to reduced switching speed and slower performance of the device. As a result a trade off between threshold voltage and supply voltage became necessary for better performance of the device.

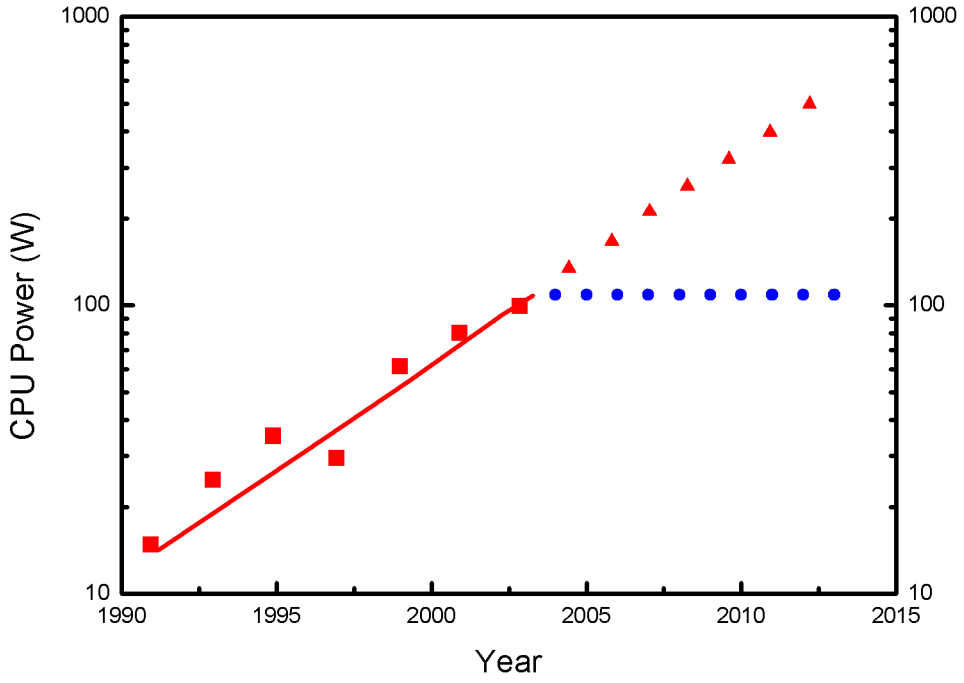


Fig. 1.1: Power dissipation in CPU for various technologies as a function of the year of introduction (Source: [10])

1.2.2 Short channel effects

When gate length becomes less than 100nm, in addition to the power consumption problem, MOS device suffers from different adverse effects such as short channel effect (SCE), hot electron effect, parasitic capacitance, leakage current etc. [11]-[13] For integrated circuits, isolation between neighboring transistors also becomes challenging at nanoscale[11]. Moreover device performance deteriorates at this scale due to velocity saturation and source velocity limit.The significant short channel effects are discussed here.

Threshold Voltage Roll-off:

The decrease of threshold voltage with decrease in gate length is a severe short channel effect which is termed as threshold voltage roll off. At reduced gate length, the charge distribution in the channel is affected by source/drain voltages. This voltage depletes a considerable amount of charge in the channel. Hence, a lower gate voltage is required to invert the

channel. As a result, short-channel MOSFETs turns on at a lower gate voltage than long-channel MOSFET [14]-[16].

Drain Induced Barrier Lowering (DIBL):

At short channel length, the longitudinal and transverse electric fields become comparable and the two electric fields interact. So, the charge in the channel is controlled by both gate and drain bias. Upon application of a high drain voltage, drain induced barrier lowering (DIBL) [17] effect occurs as the potential barrier height for channel carriers reduces due to the influence of drain electric field. The increased number of charge carrier in the channel leads to an increased off-state leakage currents. So the net effect is that DIBL causes a reduction in threshold voltage at high drain bias [18]. DIBL effect can be reduced by increasing the channel doping concentration.

Channel length modulation:

The shortening of the effective channel length at higher drain biases is known as channel length modulation [19]. At the pinch-off point, the electric fields due to drain and gate bias is comparable. A further increase in drain bias causes the pinch-off point to move away from the drain end of the channel. The net result is that the carriers are injected from the inversion layer at saturation velocity and travel to the drain. It seems as if the channel length of the device is reduced by the length of the region between pinch-off point and drain terminal. So for an increased drain bias beyond V_{dsat}, the drain current increases. As a result, transconductance increases and output resistance decreases.

Subthreshold slope:

Subthreshold slope (SS) is defined as the slope of $\log(I_d)$ vs. V_{GS} ($Vgs<V_{th}$) curve at constant V_{ds} which is expressed in decade/mV unit [20]. In short channel devices, the amount of

depletion charge controlled by the lateral electric field increases. The penetration of this source to drain electric field leads to an undesirable source-drain leakage current which is responsible for the degradation of the subthreshold drain current [21]. SS degradation can be reduced by increasing the gate capacitance and enhancing the effective carrier mobility of the channel.

Punchthrough:

Punchthrough occurs when the source and drain depletion regions overlaps. At this time, the potential barrier between source and drain reduces and carriers move from source to drain. This effect causes a conduction path independent of gate bias. Punchthrough depends on drain bias and source/drain junction depths.

Velocity saturation:

In a long-channel MOSFET the drain current increases with drain voltage until pinchoff and then remains constant at the saturation value I_{dsat}. At this region, the carrier velocity shows linear dependence on horizontal electric field. However, when the gate length is reduced the electric field in MOS devices increases. When the electric field is beyond 10^4V/cm, carrier velocities deviates from its linear characteristics. This causes the drain current to saturate prematurely at a value lower than I_{dsat} as a result of carrier velocity saturation [22]-[23]

Source-Drain Series Resistance: In long-channel device, the channel resistance is much higher than the source and drain resistance. But, in a short-channel MOSFET, the reduction of gate length reduces the channel resistance whereas source and drain resistances is increased by the reduced junction depth. This leads to current degradation at shorter gate lengths [23].

1.3 Overcoming Scaling Issues:

1.3.1 SOI FET

Researchers have tried to solve the scaling problems using strain engineering [24]. The strain engineering technique increased the device performance but the gate oxide leakage remains the same. With further scaling, gate oxide leakage current needed to be reduced. As a result, the structural modification of CMOS device became necessary. Addressing to this issues, Silicon-on-Insulator (SOI) technology was introduced to replace the bulk silicon technology[11], [25]. Depending on the channel thickness, SOI MOS can operate in fully depleted (FD) or partially depleted (PD) regimes. If the channel is so thick that the channel depletion region does not extends through the entire thickness of the channel, then the channel is said to be PD. In FD SOI, the channel depletion depth extends over the entire channel thickness. FD SOI has some advantages in comparison to PD SOI: no kink effect, better subthreshold swing, high circuit speed, low power requirements etc. [26]-[27]. Double gate SOI has reduced leakage current and better immunity to short channel effects than single gate SOI MOSFET. Thus, SOI structure allowed the scaling to continue. However, with further decrease of gate length the area of the gate oxide as well as gate oxide capacitance is reduced. But to have better control over the channel a minimum value of gate oxide capacitance is needed. This is obtained by reducing the gate oxide thickness. When SiO_2thickness goes below 1.2nm, quantum mechanical tunneling occurs [28], [29]. Any further scaling of the gate oxide increases gate oxide leakage current. Also, power consumption of the device in the off state becomes significant. This problem can be reduced by using a material that has a higher dielectric constant, known as high-k dielectric. For same oxide capacitance, use of a high-k dielectric material permits to grow a thicker gate oxide than SiO_2. The term Equivalent oxide thickness or EOT indicates how thick of a SiO_2 film is required to have the same oxide capacitance if it is used in place of high-k dielectric [29]. Use

of high-k material as gate dielectric seemed to be a successful solution up to 45nm gate length [30]. Beyond that for further scaling multi gate structures such as FinFET, DG FDSOI etc. are considered as the most attractive devices [31]-[33]. In multigate structure the electrostatics of the channel is controlled from different sides of the channel. As a result, the device offers better control over the channel with reduced leakage current, improved on state current, lower subthreshold slope (SS) and lower output conductance [34]-[35]. Due to improved performance of the devices, several FinFET technologies were demonstrated [36]-[39]. However, there are some limitations of such multigate structure. The main disadvantage was the fabrication of such 3D structure which was very challenging and costly in comparison to planar technology [40]-[46]. Self-aligned FinFET is proposed to solve this problem. Considering all these facts it seems that FinFET and SOI are two parallel solutions of the scaling challenges and best suitable for device design .

1.3.2 XOI FET:

Addressing to the scaling issue of silicon technology researchers are trying to find alternative semiconductor material with better performances. III-V materials can be considered as the perfect replacement of silicon as the channel material due to their excellent transport properties. They possess high electron and hole mobility as well as high saturation velocity [47] due to their small effective mass in r valley. Use of III-V materials in the channel would reduce the power consumption by reducing the operating voltage without compromising the switching speed. This would allow further scaling of MOS device feasible. Moreover due to their direct bandgap properties III-V materials are suitable for optoelectronic application [48]. With this persuasion, the “Compound semiconductor-on-insulator” was reported in 2010, which is also termed as XOI [49]. Due to similar device structure XOI offers all the advantages of SOI. But in sub 100nm node XOI would provide better performance than SOI by suppressing the short channel effects.

Though XOI would provide better performances than SOI devices, we need to overcome some of its limitations to utilize these devices to their full extent. One of the main issues of XOI devices is the interface quality (front oxide-channel, channel-buried oxide and buried oxide-substrate). Si and SiO_2 have good interface quality. But, III-V materials don't have any native oxide which leads to poor interface between channel and oxides. As a result, the device performance degrades because of poor interface, leaky and defective oxides. These prevent the formation of inversion layer in the interfaces. It was observed when a III-V (GaAs) MOSFET was built for the first time by Radio Corporation of America in 1965 [50]. Researchers are trying to solve this issue and assure good interface quality of XOI FET. Regarding this, Atomic Layer Deposition (ALD) technique is used to fabricate 400nm $In_{0.65}Ga_{0.35}As$ MOSFETs where a high current of 1A/mm was found with a trap density of about 1.7 $\times 10^{12}/cm^2$-eV. C-V measurement technique and conductance method is used to check the quality of the interface [51].

The quantum well (QW) structure has also attracted a lot of attention at reduced gate length. A QW transistor having $In_xGa_{1-x}As$ as the channel material has been fabricated on Si substrate [52] and good device characteristics is found for future CMOS application. But one of the major limitations of such III-V QW structure is their high gate leakage currents at different gate biases. The incorporation of a high-K (TaSiOx) and InP composite layers deposited on top of the $In_{0.7}Ga_{0.3}As$ channel reduces the gate leakage by a factor of >1000 [53]. Another issue of such III-V QW structure is its series resistance that is about 2~3 times of today's Si MOSFET [54], [55]. To have better device performance this issue needs to be solved and researchers are working on it.

For CMOS application both p type and n type MOS is necessary. So electron and hole mobility is a big concern in such type devices. Among all other III-V materials, antimonides based material have good electron and hole mobility namely InSb and GaSb respectively

[56]. Recently, InGaSb based p channel MOSFET for 150µm gate length has been reported with reduced gate leakage current and source/drain resistance while ensuring high mobility [57]. But for sub 20nm regime the transport becomes ballistic and the concept of mobility does not work. So, at this ultra scaled limit device performance does not deteriorate due to mobility. But the control of gate over the channel seems to be a challenge at this limit.

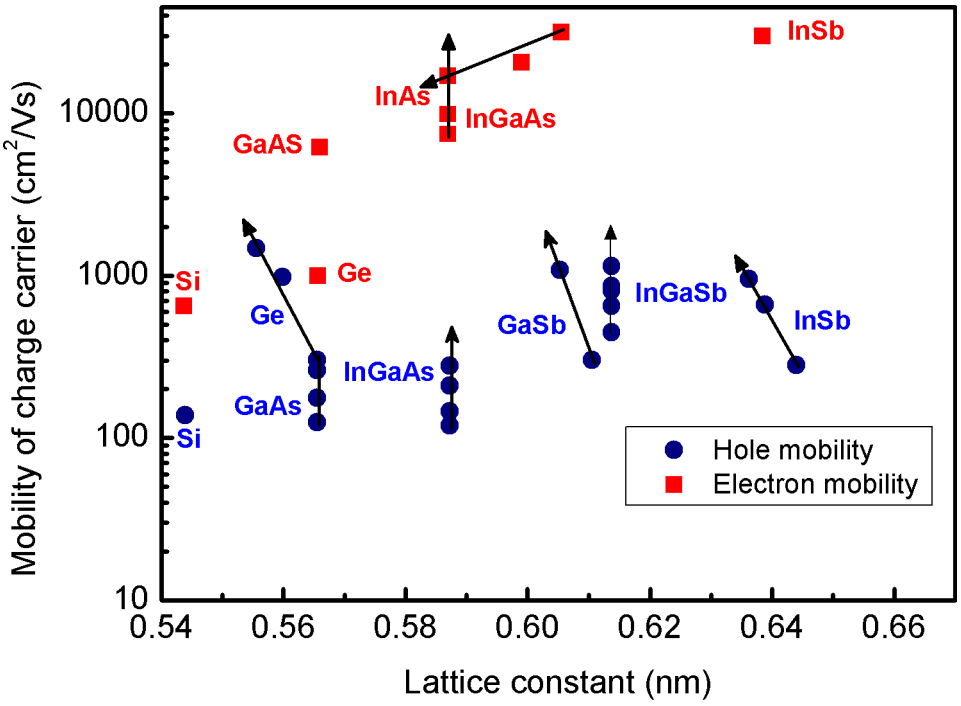


Fig. 1.2: Electron and hole mobility's of various III-V compound semiconductors (Source: del Alamo MIT [55])

XOI FET's are becoming very popular due to their attractive features in ultra-scaled and ultra-low-power devices. C-V measurement technique is also used to study the interface quality, hence to understand the device electrostatics behavior. By comparing an experimental and an ideal C-V curve- interface quality, threshold voltage shift etc. can be understood. C-V models are also used for device parameter extraction of MOS devices.

Compact analytical models are necessary for fast and accurate estimation of device characteristics in circuit simulations. Moreover compact models provide insight into device

response when device parameters or excitations are varied. Predictability is an important requirement in a compact analytical model. Quantum mechanical and other complex physical phenomena determine the characteristics of modern semiconductor devices owing to the nanoscale dimensions and bandgap engineering. Thus empirical models fail to predict the characteristics of such devices. In this work, an analytical model is developed to study the C-V characteristics of ultra scaled XOI FET in terms of different device parameters.

1.4 Thesis objectives:

The main objective of this thesis is to develop an analytical C-V model for III-V-on-Insulator FET. The specific objective of this work includes:

- To develop an analytical model that explains the C-V characteristics of ultra scaled XOI FET
- To study the channel thickness dependent shifts in C-V curves
- To investigate the effect of doping and channel material composition on the C-V characteristics
- To study the effect of temperature on C-V characteristic
- To determine the threshold voltage of ultra thin body XOI FET

The final goal is to validate the model through a comparison between the results obtained from analytical model with those of numerical simulation obtained using Silvaco Atlas.

1.5 Thesis layout:

Chapter 2 briefly explains the necessity of C-V models for device design. The use of C-V models for device parameter extraction is studied here. After that, previously reported III-V materials based C-V models are also discussed.

In chapter 3, the physical structure of the device (XOI nFET) and different device parameters used in this analysis are summarized. The mathematical formulation of the quantum mechanical effects and device electrostatics of ultra scaled XOI FET is discussed here that explains the C-V characteristics of the device at quantum regime.

Chapter 4 describes the results obtained from the analytical model. C-V curve of XOI FET is studied in terms of different device parameters such as channel thickness, channel material composition etc. Effect of doping and temperature on the shift of C-V curve is also studied. At last, the results obtained from the analytical model have been compared with the numerical results.

Finally, the concluding remarks and future works are presented in chapter 5.

Chapter 2

C-V Analysis: Importance and Models

Chapter Outlines

- Introduction
- Necessity of C-V models
- C-V models for bulk and SOI FET
- C-V models for III-V FET

2.1 Introduction

C-V measurement is a fundamental technique for MOSFET characterizations and is very crucial in providing device information. Thin oxide causes tunneling which increases the gate leakage current owing to the low impedance of the MOS capacitor. This causes capacitance attenuation in ultra thin gate MOS devices which can be overcome using shorter channel lengths. But, shorter channel length introduces different short channel effect that degrades device performance. Also, due to various parasitic capacitances, the measurement of intrinsic gate capacitance becomes difficult.C-V models are important in determining gate capacitance of MOS devices which is necessary for analyzing device performance.

2.2 Necessity of C-V model

Using C-V characteristics different device parameters (i.e. oxide thickness, channel thickness etc.) can be extracted [58], [59]. In scaled down devices, interface quality plays a very vital role. Normally, we assume that there are no trap charges at Si/SiO_2 interface and this interface is electrically neutral. But in real devices, interfaces are far from electrically neutral because they are affected by fixed oxide charges, mobile ionic charges and positive or negative charges at the interface. C-V methods are widely used to determine the interface quality of MOS devices [60].

2.2.1 Interface states

The interface charges locate in close proximity to channel-oxide interface and have an energy distribution along the bandgap of the material. The position of these interface states are fixed.The probability of an electron or hole to be trapped within these states depends on the position of the fermi level. When channel potential changes, the position of the fermi level

and the probability of charge occupation within the interface state also changes. When a state becomes positively charged by donating an electron, it is called a donor state and when it becomes negatively charged by accepting an electron, it is called an acceptor state. Every interface has both donor state and acceptor state. The charge neutrality level (CNL) is used to express the summation of these states on an equivalent interface state density distribution. When the Fermi level coincides with the CNL, the interface states are neutral. Interface states above CNL are acceptor states and below CNL are donor states. So, when the fermi level is above CNL, the occupied states are negatively charged and when E_F is below E_{CNL} the occupied states are positively charged.

2.2.2 Effect of interface states in III-V materials

The effect of interface states are significant in III-V on Insulator devices as III-V material does not have any native oxides with good stability, low leakage and high breakdown fields. So, suitable gate dielectrics must be developed, which must form a stable interface for transistor fabrication process. The dielectric should have a high dielectric constant, low gate leakage and have a low interface trap state density. Among these characteristics, achieving low interface trap density is very challenging. High interface trap densities can cause a shift in fermi level, threshold voltage and on drive current. As a result the control over the charge carriers in the channel is lost. For this reason, study of interface states is necessary. In 1960, several methods were developed to determine trap state density D_{it} and the trap level energy position for Si/SiO_2 interfaces [61]. However, dielectrics/III-V interfaces has low conduction band DOS, different minority carrier response time and high trap density with an energy distribution which is different from Si/SiO_2 interfaces. Recently a model has been proposed to study the origin of GaAs gap states based on the concept of metal-induced gap states (MIGS) [62], [63]. In this model, it is suggested that $In_{0.53}Ga_{0.47}As$ based n-type FETs has higher on-state current and lower sub-threshold slope compared to GaAs based n-type FETs.

The position of the charge neutrality level and larger density of metal-induced gap states (MIGS) below the conduction band edge deteriorates the performance of GaAs based n-type FET. But, there is another model that suggests that there are no MIGS in the semiconductor bandgap next to a wider bandgap oxide [64]. So, interface states at the III-V semiconductor/oxide interface cannot be due to MIGS, but originate from the native interface defects. In case of GaSb and InSb the CNL lies well below the Fermi level leading to a negatively charged acceptor state [65]. Using linear interpolation [65] of the tight binding study CNL of InGaSb is found to be 0.398eV below the conduction band minima. Using these conditions the value of D_{it} can be extracted. D_{it} concentration greatly depends upon the processing and passivation technique. Ohtakeet et al. reported a processing technique that extract a D_{it} value of $2*10^{12}eV^{-1}cm^{-2}$ for HfO2/GaSb interface [66]. Passivation using $(NH_4)_2S$ offers uniform distribution of D_{it} from CNL to CBM [67].

2.2.3 D_{it} Extraction

Various methods are used for the extraction of D_{it}, such as interpretation of shifts in the capacitance-voltage (C-V) curves with gate metal work function [68,69], the conductance method [70], the Terman high-frequency capacitance method [71], the combined high-low frequency capacitance (Castagné–Vapaille) method [72], the Berglund integral [68], and the fermi level efficiency method [73]. Using these methods the reported values of D_{it} is found to vary from 10^{11} cm^{-2} eV^{-1} to exceeding 10^{13} cm^{-2} eV^{-1}. Among these methods, conductance and capacitance based methods are normally used to quantify D_{it}.

2.2.3.1 Conductance method

In this method the interface trap density(D_{it}), and the trap level energy position (E_T) are determined by analyzing the loss occurred due to the change in the trap level charge state. The equivalent parallel conductance G_p is given by [70]:

$$G_p = \frac{\omega^2 C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \tag{2.1}$$

Here ω is the angular frequency ($\omega = 2\pi f$), C_{ox} is the gate oxide capacitance, G_m and C_m are measured conductance and capacitance respectively. Interface trap charges in close proximity of fermi level can change their occupancy. The loss is maximum when the interface trap charges are in resonance with the applied ac signal. The trap time constant determines the frequency dependent response of the trap charges which is given by [74]

$$\tau = \frac{\exp[\Delta E/kT]}{\sigma v_{th} D_{dos}} \tag{2.2}$$

where ΔE is the energy difference between trap level and majority carrier band edges , $\sigma$is the capture cross section of the trap, $v_{th}$is the average thermal velocity of the majority carriers, D_{dos} is the effective density of state (DOS) of the majority carrier band, $k$is the Boltzmann constant and $T$is the temperature. If the surface potential fluctuations are neglected, then the D_{it}can be estimated from the normalized parallel conductance peak,$(G_p/\omega)_{max}$ [74]

$$D_{it} = \frac{2.5}{Aq}\left(\frac{G_p}{\omega}\right)_{max} \tag{2.3}$$

Similarly, the position of the trap charges,$E_T$in the band gap can be determined from "(2.2)".

The conductance method has the advantage of determining D_{it} directly from the experiment. Also the amount of band bending and fermi level movement with gate bias can also be observed directly. Because, they are correlated with the shift in the frequency of the maximum normalized conductance peak as a function of gate bias.

2.2.3.2 Capacitance-Voltage (C-V) based method

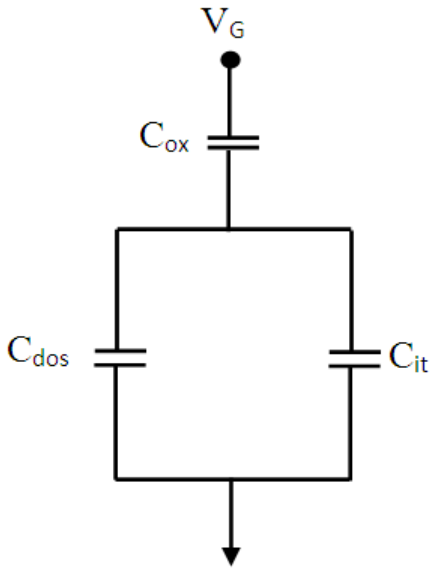


Fig. 2.1: Equivalent circuit of a MOS capacitor showing oxide capacitanceC_{ox}, interface trap capacitance C_{it} and semiconductor capacitance C_{dos}

Fig. 2.1 shows the equivalent circuit of a MOS structure. The total capacitance can be given by

$$\frac{1}{C_{tot}} = \frac{1}{C_{ox}} + \frac{1}{C_{it} + C_{dos}} \tag{2.4}$$

D_{it} can be known from C_{it} if C_{dos} and C_{ox} are known. Using low frequency C-V measurement techniques C_{tot} is calculated where the frequencies are so low that the trap charges can follow the ac signal. By increasing the gate voltage and measuring the displacement current, D_{it} ($C_{it} = qD_{it}$) is then calculated from"(2.4)".

$$D_{it} = \frac{1}{q}\left(\frac{C_{ox}C_{tot}^{lf}}{C_{ox} - C_{tot}^{lf}} - C_{dos}\right) \tag{2.5}$$

In high frequency C-V measurement method the frequencies are so high that the trap charges cannot follow the ac signal ($C_{it} = 0$). C_{ox} can be eaily determined experimentally using

channel thicknesses. So, C_{dos} can be calculated from"(2.4)". After using high and low frequency method D_{it} can be calculated as (Castagné–Vapaille method) [75]

$$D_{it} = \frac{1}{q}\left(\frac{C_{ox}C_{tot}^{lf}}{C_{ox} - C_{tot}^{lf}} - \frac{C_{ox}C_{tot}^{hf}}{C_{ox} - C_{tot}^{hf}}\right) \tag{2.6}$$

The trap level position can be determined by knowing the band bending as a function of gate voltage. The band bending can also be calculated using the Berglund integral [76]

$$\psi_s = \psi_s{}^o + \int_{V_G^0}^{V_G} (1 - \frac{C_{tot}^{lf}}{C_{ox}})\, dV_G \tag{2.7}$$

The Terman method is used to extract D_{it} from high frequency C-V curves [77]. Due to high frequency, there are no contributions of interface trap charges. The only influence of interface traps is the stretch-out of C-V curves as the occupancy of trap charge changes with gate bias. The stretch-out quantity is then compared with an ideal C-V curve.

$$D_{it} = \frac{C_{ox}}{q}\left[(d\psi_s/dV_G)^{-1} - 1\right] - C_{dos} \tag{2.8}$$

Forextracting D_{it}, the low and high frequency experiments should be done at true low and high frequencies so that all trap charges contributes to the low frequency and no trap charge should contribute to high frequency.

2.2.4 Limitations of C-V based methodsforD_{it}extraction

In case of Si/Sio_2 interface, C-V curves are calculated using charge carrier densities at the semiconductor surface using Boltzman statistics which is also known as classical approximation. In this method the fermi level remains within the band gap for all gate biases.

But owing to the low effective mass of III-V materials, they have a small conduction band DOS. So, at high C_{ox} the high electric field at the semiconductor causes the Fermilevel move within the conduction band. As a result classical approximation fails.

i) Berglund integral

As there are considerable amount of band bending when the Fermi level resides inside the conduction band, the Berglund integral becomes intractable in such cases. The band bending in accumulation contributes to the total band bending determined from the Berglund method and has to be subtracted if the fermi level movement inside the band gap is to be reported. This issue makes Berglund method less suitable for high-k/III-V interfaces.

ii) High-low frequency (Castagné–Vapaille) method

Figure 2.2 shows that the value of D_{it} obtained from the Castagné–Vapaille (HF-LF) method are smaller than those obtained using the Terman method. The reason is that the frequency values selected for low (100Hz) and high (100MHz) frequencies are not true values of low and high frequency curves. As traps close to the band edge respond first, the ac contribution of interface traps reduces the apparent stretch-out of the measured curve. As a result, the D_{it} value is underestimated due to the increase in slope of the measured C-V curve.

iii) Terman method

The Terman method used for D_{it} extraction has two input parameters needed to calculate the ideal C-V curve, namely the dopant concentration and the oxide capacitance. If the doping concentration is right than the correct value of D_{it} is obtained, even at large negative band bending. But an erroneous low value of doping concentration causes an overestimated value of Dit and the extracted band bending suggests fermi level pinning. On the other hand, an erroneous high value of doping concentration causes an underestimation of D_{it} as the ideal

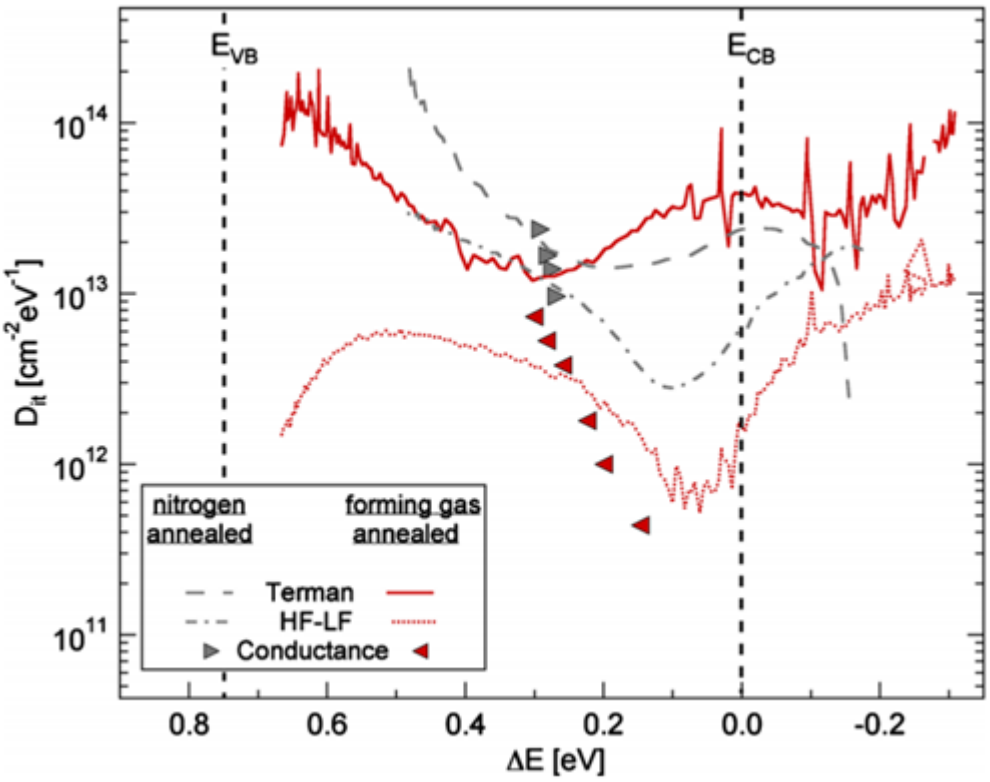


Fig. 2.2: Extractions of interface trap density of $HfO_2/In_{0.53}Ga_{0.47}As$using Terman, HF-LF and conductance method [60].

C-V curve is more stretched out. In inversion, the Terman method is not applicable as the slope of the high-frequency C-V curve is zero. So, the inverse stretch-out $(d\psi_s/dV_G)^{-1}$diverges and along with it the apparent D_{it}. The oxide capacitance also has an impact in D_{it} extraction. Large values of C_{ox} undersestimates the band bending and overestimates D_{it} inside the conduction band.

2.3 C-V models for bulk and SOI FET

2.3.1 Bulk MOS

In bulk MOSFET the gate capacitance is determined as a series combination of oxide capacitance and semiconductor capacitance.

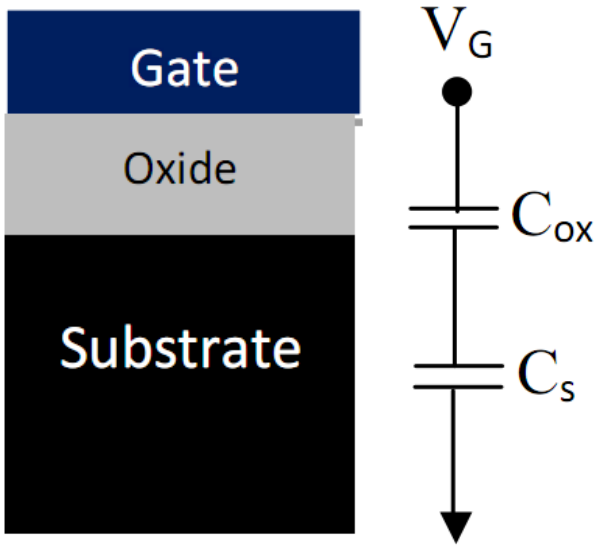


Fig. 2.3: Bulk MOS structure with equivalent capacitance model

The gate capacitance,C_g is given by

$$C_g = \frac{`1}{\frac{1}{C_{0x}} + \frac{1}{C_s}} \tag{2.9}$$

whereC_{0x} is the oxide capacitance and C_s is the semiconductor capacitance.

In accumulation region, as the majority charge carriers accumulates to the surface, $C_s$becomess much higher thanC_{0x}. So, the oxide capacitance dominates.

$$C_g = C_{0x} \tag{2.10}$$

In depletion region, the channel is depleted of majority carrier and including the depleted capacitance, C_g is given by

$$C_g = \frac{\varepsilon_{0x}}{t_{ox} + \frac{\varepsilon_{0x}}{\varepsilon_s} W} \tag{2.11}$$

With further increase of gate voltage the channel gets inverted. At that time the oxide capacitance dominates again.

$$C_g = C_{0x} \tag{2.12}$$

2.3.2 SOI FET

As the channel length gets reduced, modification of device structure became necessary for improved device performance. SOI MOSFETs are two types- partially depleted MOS and fully depleted MOS. In partially depleted MOS the front surface and back surface potentials are not mutually coupled. So they can be considered as two independent MOS that work like bulk MOSFET. As the channel length is reduced the channel becomes depleted of majority carriers and the structure is termed as fully depleted MOSFET. In FD SOI structure, the space charge layers are coupled so the front and back surface potential becomes coupled. In case of SOI structure, the overall capacitance is taken here as a series combination of front oxide, back oxide, channel and substrate capacitance as shown in Fig. 2.4.

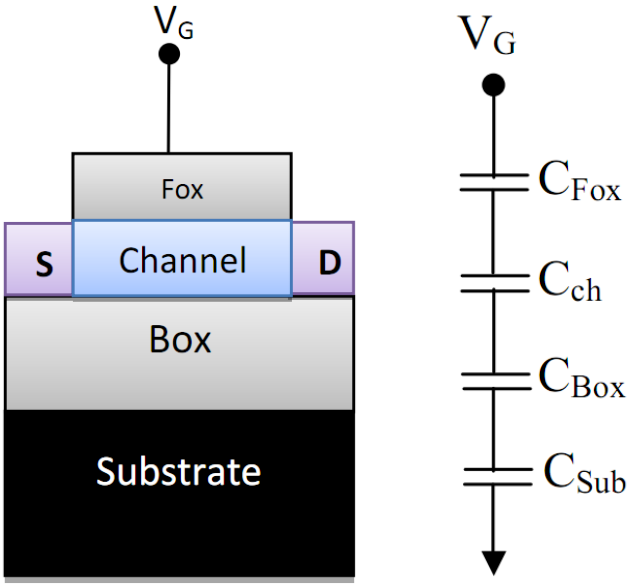


Fig. 2.4: SOI FET structure and equivalent capacitance model

If total capacitance is taken as C_T then,

$$\frac{1}{C_T} = \frac{1}{C_{Fox}} + \frac{1}{C_{ch}} + \frac{1}{C_{Box}} + \frac{1}{C_{sub}} \tag{2.13}$$

$$C_{Fox} = \frac{\varepsilon_{Fox}}{t_{Fox}} \tag{2.14}$$

$$C_{ch} = \frac{dQ_{ch}}{dV_G} \tag{2.15}$$

$$C_{Box} = \frac{\varepsilon_{Box}}{t_{Box}} \tag{2.16}$$

$$C_{sub} = \frac{dQ_{sub}}{dV_G} \tag{2.17}$$

Here ε_{Fox} and ε_{Box} are front and back oxide permittivities and t_{Fox} and t_{Fox} represents the thicknesses of front and back oxides respectively. Q_{ch} and Q_{sub} represent the channel charges at the channel and substrate, respectively.

At reduced gate length, the SCE becomes severe. So, researchers are trying to find alternative materials that can replace silicon and show good device performance. III-V materials are strong candidate for this.

2.4 C-V models for III-V FET

Because of the low effective mass of III-V based devices they show quantization effect. The gate capacitance of III-V based MOS devices can be explained by the inversion layer capacitance model. The inversion layer capacitance model consists of

i) Quantum capacitance model and

ii) Centroid capacitance model

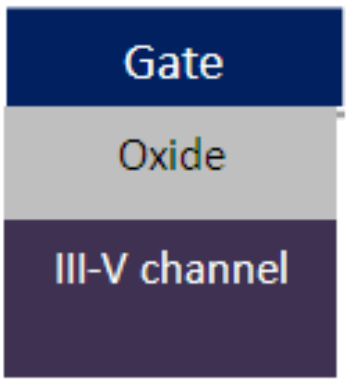
2.4.1 Inversion layer capacitance model

In this model the gate capacitance is taken as a series combination of oxide capacitance C_{ox} and inversion layer capacitance C_{inv}. The small effective mass of III-V materials causes the energy level to be quantized. The contribution of each quantized subband is taken as a parallel combination of each capacitance. For each subband, the inversion layer capacitance consists of the quantum capacitance C_Q and the centroid capacitance C_{cent}. In this model it is assumed that there is no doping underneath the channel. Here,

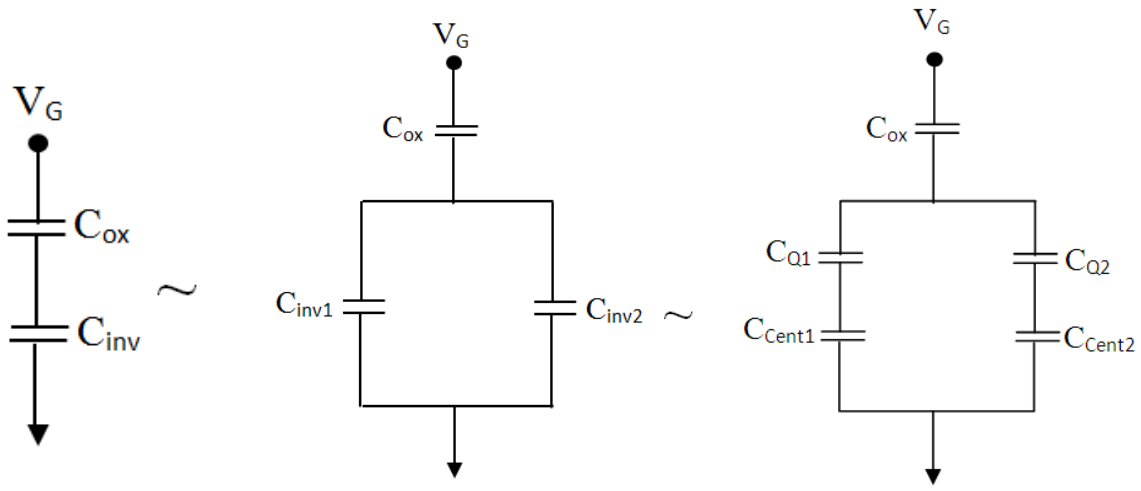
$$C_{inv} = \sum_i \left(\frac{1}{C_{Q\_i}} + \frac{1}{C_{cent\_i}}\right)^{-1} \tag{2.18}$$

where,

$$C_{Q\_i} = \frac{4\pi m^* q^2/h^2}{1 + exp(E_i - E_f)/kT} \tag{2.19}$$



(a)



(b)

Fig. 2.5: (a) III-V MOS structure (b)Equivalent gate capacitance circuit model for III-V MOS structure.

$$C_{cent\_i} = C_{Q\_i}\frac{\delta(E_f - E_i)}{\delta(E_i - E_c)} \tag{2.20}$$

So, the overall capacitance of the device can be evaluated if the location of each subband energy and Fermi levels are known. This model is solved numerically for all subbandenergy level by solving 1 D Poisson-Schrodinger.

2.4.1.1 Quantum capacitance model

Quantum capacitance is very important for low density of state system. S. Luryi first introduced the concept of quantum capacitance [60]. Quantum capacitance comes into consideration when a 2DEG is formed in semiconductor surface or interface. Since the DOS is finite in the quantum well, the Fermi level needs to move up when the charge of the quantum well increases. This movement of Fermi-level requires energy and this conceptually corresponds to quantum capacitance. To induce channel charge in MOS structure the amount

of energy needed is given by $\frac{Q_S^2}{2C_{ox}} + \frac{Q_S^2}{2C_Q}$ where Q_S is the total charge in the channel and $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ .The first term indicates the energy required for the electric field in the oxide layer and the second term is for the energy required to form a 2DEG in semiconductor layer. Normally, the insulator capacitance is smaller in contrast to quantum capacitance. So, the first term dominates in determining the gate capacitance. But as the devices are scaled down the quantum capacitance becomes comparable to oxide capacitance in nanometer regime.

III-V materials have smaller effective mass than silicon and, hence lower DOS. In a 3D bulk structure, the electron effective masses are considered to be m_x , m_y and m_z which corresponds to the direction of movement. However, in 2D quantum well structure, depth direction is the direction of confinement and only parallel movement in the quantum well plane is allowed. In such quantum well we have two different kinds of effective mass: in-plane effective mass and perpendicular effective mass. The in plane effective mass is responsible for the transport property in the quantum well plane and determines 2D DOS. On the other hand, the perpendicular effective mass determines the subband energy levels.

In weak inversion region when $(E_f < E_i)$, the quantum capacitance is negligible and in strong inversion region $(E_f > E_i)$, the quantum capacitance is equal to $4\pi m^* q^2/h^2$. The quantum capacitance is sometimes referred to as the average DOS at the Fermi-level

2.4.1.2 Centroid capacitance model

The charges in the quantum well distributes as a bell shape distribution in the channel. Therefore, the physical distance of each charge is different from the metal gate. This effect is important in determining the total inversion layer capacitance of MOS devices. Furthermore, due to confinement in the quantum well, the centre of the charge distribution is

situated far from the barrier interface. The common method to include the charge distribution effect into the gate capacitance model is to determine an average charge distance from the interface between the barrier and the channel which is quite complicated [79]-[80]. Using inversion layer capacitance model, the centroid capacitancecomponent can be calculated if the location of E_i and E_c with respect to E_f are known.

Some compact models have been proposed for III-V materials based symmetrical double gate MOS devices [81]-[82]. But, there are no such models for asymmetrical devices, where the effect of BOX capacitance becomes comparable to channel capacitance. So, the box capacitance becomes very significant. In the next chapter, we are proposing a capacitance model for III-V materials based asymmetrical double gate MOS devices.

Chapter 3

Proposed C-V model

Chapter Outlines

- Introduction
- Device structure
- Mathematical model
- Threshold voltage model

3.1 Introduction

Compact models are necessary for fast estimation of device characteristics in circuit simulations. Predictability is an important requirement for any effective compact model. Quantum mechanical and other complex physical phenomena determine the characteristics of modern semiconductor devices owing to the nanoscale dimensions and bandgap engineering. Thus empirical models fail to predict the characteristics of such devices. The motivation of this work is to develop a physics based general analytical model to simulate the gate C-V characteristics of XOI FET.

3.2 Device structure

The XOI device structure studied in the research work is shown in Fig. 3.1. The device parameters are shown in the following table:

Table 3.1: Device parameters of UTB XOI FET

Symbol	Description	Value
t_{ch}	Channel thickness	7nm – 20nm
$In_{0.3}Ga_{0.7}Sb$ or $InAs_{0.7}Sb_{0.3}$	Channel material	--
t_{Fox}	Front oxide thickness (HfO_2)	10nm
t_{Box}	Buried oxide thickness (SiO_2)	50nm
N_D	Channel doping	$1*10^{17}$ cm^{-3}
k	Boltzman constant	$1.38*10^{-23}$ JK^{-1}
T	Temperature	300K

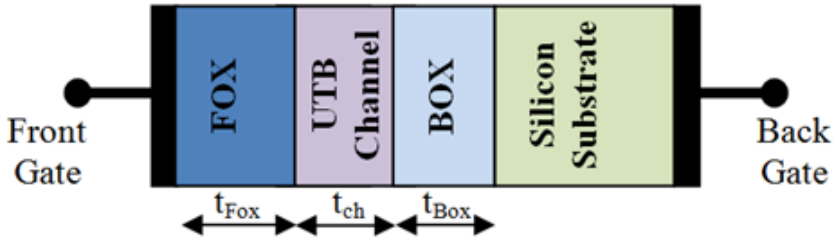


Fig. 3.1: Schematic diagram of XOI FET.

3.3 Mathematical model

The main objective of this study is to develop a general analytical compact model to express the gate voltage dependent capacitance characteristics of ultra-thin body (UTB) XOI FET. In case ofUTB XOI FET, the C-V characteristic is differentbecause of the discrete energy levelsof such devices due to quantum confinement effect. For getting insight to the C-V characteristic, the quantum mechanical charge in different subbands of the channelneeds to becalculated [83]. To ensure charge equilibrium condition, the gate charge must be balanced by the quantum mechanical charge found at the channel and the substrate of the device [84]. As we have a thick buried oxide layer and the substrate is assumed to be undoped, the probability of substrate inversion and thereby, the carrier confinement in the substrate is assumed to be low. If the effect of substrate charge is considered negligible, the effective capacitance of the device can be expressed by,

$$C_G = -\frac{dQ_{ch}^{QM}}{dV_G} \tag{3.1}$$

The quantum mechanical charge, Q_{ch}^{QM}at the channel can be determined from the density of states (DOS) at the channel and Fermi Dirac distribution. But this calculation requires some careful attention. The strong quantum confinement along the thickness (x direction in Fig. 3.2(a)) discretizes the energy level of the channel. Two such discrete energy levels are shown in Fig. 3.2(a) by$E_1$and E_2. Note that other directions (y and z) do not impose any quantum confinement effect to the transport of electrons. Thus, the solution of Schrodinger equation along these directions will be plane wave, that would ultimately give a two dimensional (2D) DOS for each discrete energy level.

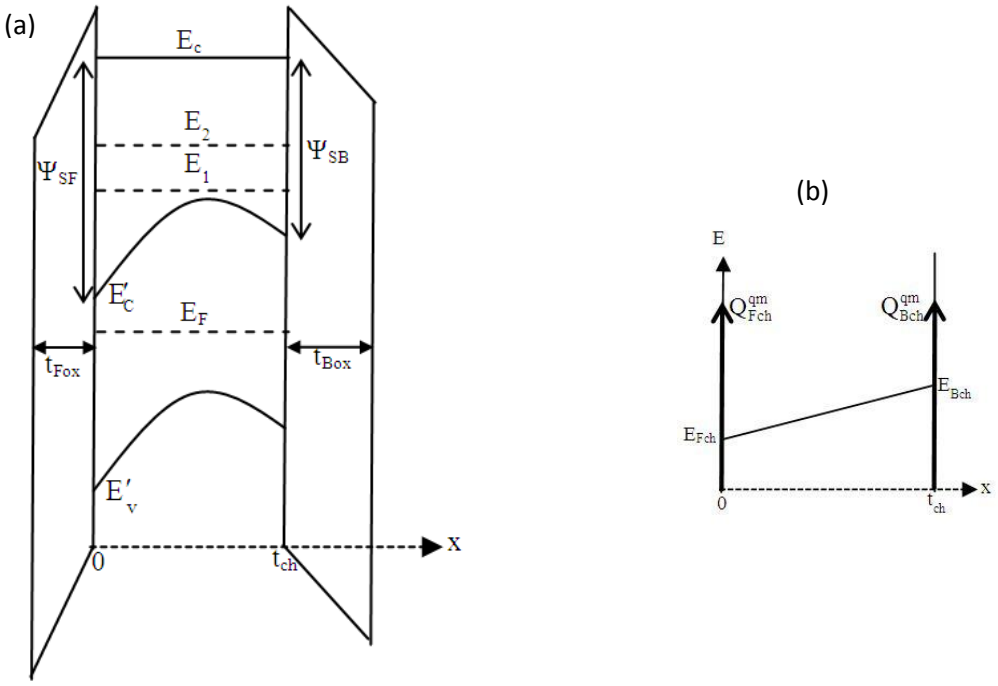


Fig. 3.2: Potential and field distributions of XOI FET structure (a) Potential distribution and (b) field distribution.

For the i^{th} discrete energy level E_i, if the number of energy states (arises from 2D plane wave) in the energy between E and $E + dE$ be $N(E)$, then using 2D DOS the number of electrons can be obtained from

$$n = \frac{4\pi g m^* kT}{h^2} ln\left[1 + e^{(E_F - E_{min})/kT}\right] \tag{3.2}$$

where g is the number of equivalent minima in conduction band, m^* is the effective mass, k is the Boltzmann constant, h is the Planck's constant, T is the temperature and E_F is the Fermi level.

Since the channel potential changes with gate bias, all the eigen levels as well as the conduction band minima goes downward. When an energy eigen level goes below E_F, that level gets populated. The minimum energy required to populate the i^{th} subband can be given by

$$E_{min} = E_C^{'} + E_i = E_C - q\psi_{ch} + E_i \tag{3.3}$$

where ψ_{ch} is the potential that moves the bottom of the conduction band from E_C to $E_C^{'}$.

Using equation "(3.2)" and"(3.3)", the number of electrons per unit area in i^{th} subband can be determined and then summing over all the subbands, we get total charge per unit area

$$Q_{ch}^{QM} = -\frac{4\pi g m^* qkT}{h^2} \sum_i ln\left[1 + e^{(E_F - E_C + q\psi_{ch} - E_i)/kT}\right] \tag{3.4}$$

For the device structure shown in Fig. 3.1, the depth of quantum well is found to be greater than 4eV when $In_{0.3}Ga_{0.7}Sb$ is used in the channel. This can be considered as infinite quantum well even for the lowest channel thickness (7nm), as long as up to 2nd eigen level is taken into consideration. Energy of higher subbandsare too high, and that is why infinite well approximation remains no longer valid. In our case, E_i(up to 2nd eigen level) is calculated solving Schrodinger equation in the infinite well approximation,

$$E_i = \frac{i^2 h^2}{8 m^* t_{ch}^2} \tag{3.5}$$

where t_{ch} is the channel thickness. Using "(3.1)" and "(3.4)" the quantum capacitance, C_G can be expressed by

$$C_G = \frac{4\pi g m^* q^2}{h^2} \sum_i \frac{e^{(E_F - E_C + q\psi_{ch} - E_i)/kT}}{1 + e^{(E_F - E_C + q\psi_{ch} - E_i)/kT}} \frac{d\psi_{ch}}{dV_G} \tag{3.6}$$

In case of the 1st and 2nd subbands population the values of i are equal to 1 and 2, respectively.

To buildup the gate voltage dependent total capacitance relationship, we have to find a correlation between the channel potential and gate voltage. As the channel is doped with n type impurity using Gauss law we can write

$$\frac{d\xi}{dx} = \frac{q}{\varepsilon_{ch}}(N_D - n) \tag{3.7}$$

Here N_D is the doping concentration, ε_{ch} is the dielectric constant of the channel material and ξ is the electric field. For fully depleted XOI, the quantum charge inside the channel is distributed along the thickness of the channel [84]. To avoid the complexity of mathematical calculation we adopt the delta-charge approximation, i.e. the distributed charge is assumed to be concentrated at FOX-channel interface $(x = 0)$ and BOX-channel interface $(x = t_{ch})$ as shown in Fig. 3.2(b). Therefore inside the channel "(3.7)" can be rewritten as

$$\frac{d\xi}{dx} = \frac{q}{\varepsilon_{ch}} N_D [0^+ < x < t_{ch}^-] \tag{3.8}$$

After integrating "(3.8)" we have,

$$\xi_{Bch} - \xi_{Fch} = \frac{q}{\varepsilon_{ch}} N_D t_{ch} \tag{3.9}$$

ξ_{Fch} and ξ_{Bch} are the electric field at the FOX-channel interface and channel-BOX interface respectively.

Equation "(3.9)" suggests that the channel electric field varies linearly, forming a trapezoidal nature as shown in fig. 3.2(b). Integrating this linearly varying field, we get the potential difference that is actually given by the area under the trapezoid.

If ψ_{sf} is the front surface potential and ψ_{sb} is the back surface potential of the channel, then

$$\psi_{sf} - \psi_{sb} = \frac{1}{2}(\xi_{Fch} + \xi_{Bch}) t_{ch} \tag{3.10}$$

With the combination of "(3.9)"and "(3.10)" the front and back surface electric fields can be expressed by

$$\xi_{Fch} = \frac{\psi_{sf} - \psi_{sb}}{t_{ch}} - \frac{qN_D}{2\varepsilon_{ch}} t_{ch} \tag{3.11}$$

and

$$\xi_{Bch} = \frac{\psi_{sf} - \psi_{sb}}{t_{ch}} + \frac{qN_D}{2\varepsilon_{ch}} t_{ch} \tag{3.12}$$

As the electric flux is continuous in front oxide/channel interface, we can relate the electric field inside the FOX (ξ_{Fox}) with the channel electric field (ξ_{Fch}) while taking the quantum charge into consideration

$$\varepsilon_{Fox}\xi_{Fox} = \varepsilon_{ch}\xi_{Fch} - Q_{Fch}^{QM} \tag{3.13}$$

where $\xi_{Fox} = \frac{V_{FG} - \phi_{msf} - \psi_{sf}}{t_{Fox}}$

Rearranging "(3.13)" the front surface electric field can be written as

$$\xi_{Fch} = \frac{C_{Fox}}{\varepsilon_{ch}}\left(V_{FG} - \phi_{msf} - \psi_{sf}\right) + \frac{Q_{Fch}^{QM}}{\varepsilon_{ch}} \tag{3.14}$$

where $C_{Fox} = \frac{\varepsilon_{Fox}}{t_{Fox}}$

Here V_{FG}, ϕ_{msf} and C_{Fox} are front gate voltage, front gate flat band potential and FOX capacitance, respectively.

Similarly, the back surface electric field can be written as

$$\xi_{Bch} = \frac{C_{Box}}{\varepsilon_{ch}}(\psi_{sb} - V_{BG} + \phi_{msb}) - \frac{Q_{Bch}^{QM}}{\varepsilon_{ch}} \tag{3.15}$$

where $C_{Box} = \frac{\varepsilon_{Box}}{t_{Box}}$

Here V_{BG}, ϕ_{msb} and C_{Box} are back gate voltage, back gate flat band potential and BOX capacitance, respectively.

Substituting "(3.11)" into "(3.14)" the front gate voltage V_{FG} can be given by

$$V_{FG} = \phi_{msf} + \psi_{sf} + \frac{\varepsilon_{ch}(\psi_{sf} - \psi_{sb})}{C_{Fox}\, t_{ch}} - \frac{Q_{Fch}^{QM}}{C_{Fox}} - \frac{qN_D}{2C_{Fox}} t_{ch} \tag{3.16}$$

Similarly, the back gate voltage V_{BG} can be given by

$$V_{BG} = \phi_{msb} + \psi_{sb} - \frac{\varepsilon_{ch}(\psi_{sf} - \psi_{sb})}{C_{Box}\, t_{ch}} - \frac{Q_{Bch}^{QM}}{C_{Fox}} - \frac{qN_D}{2C_{Box}} t_{ch} \tag{3.17}$$

with the combination of "(3.12)" and "(3.15)".

Equations "(3.4)", "(3.16)", and "(3.17)"are coupled with each other through the quantum mechanical charge. Therefore,these equations cannot be solved exactly independently. At this stage we neglect this coupling for the time being.When $V_{BG} = 0V$, putting $Q_{Bch}^{QM} = 0$ and using"(3.17)"we get,

$$\psi_{sb} = \frac{\frac{\varepsilon_{ch}\psi_{sf}}{C_{Box}\, t_{ch}} + \frac{qN_D}{2C_{Box}} t_{ch} - \phi_{msb}}{1 + \frac{\varepsilon_{ch}}{C_{Box}\, t_{ch}}} \tag{3.18}$$

Putting this value into "(3.16)" we get

$$V_G = V_{FG} = \phi_{msf} + \psi_{sf} + \frac{\varepsilon_{ch}\psi_{sf}}{C_{Fox}\, t_{ch}} - \frac{\varepsilon_{ch}}{C_{Fox}\, t_{ch}} \left(\frac{\frac{\varepsilon_{ch}\psi_{sf}}{C_{Box}\, t_{ch}} + \frac{qN_D}{2C_{Box}} t_{ch} - \phi_{msb}}{1 + \frac{\varepsilon_{ch}}{C_{Box}\, t_{ch}}} \right) - \frac{Q_{Fch}^{QM}}{C_{Fox}} - \frac{qN_D}{2C_{Fox}} t_{ch} + \psi_{SCF} \tag{3.19}$$

Note that a self-consistent potential $\psi_{SCF=}\alpha\, Q_{Fch}^{QM}/C_{ch}$ is added on the right hand side of "(3.19)", to balance the twosides by offsetting the error induced due to neglecting the coupling of potential equations with the channel charges. Here $C_{ch} = \varepsilon_{ch}/t_{ch}$, and α is a self-consistent parameter. Value of α is determined from a comparison between results obtained from analytical calculation and numerical simulation using Silvaco Atlas simulator. As the value depends on the channel material as well as on the thickness of the channel, α must be calibrated for each particular device technology by comparing with either TCAD or experimental results. Note that its value does not have any dependency on the doping concentration. Figure 3.3 shows the value of α for InGaSb and InAsSb at different channel thicknesses.

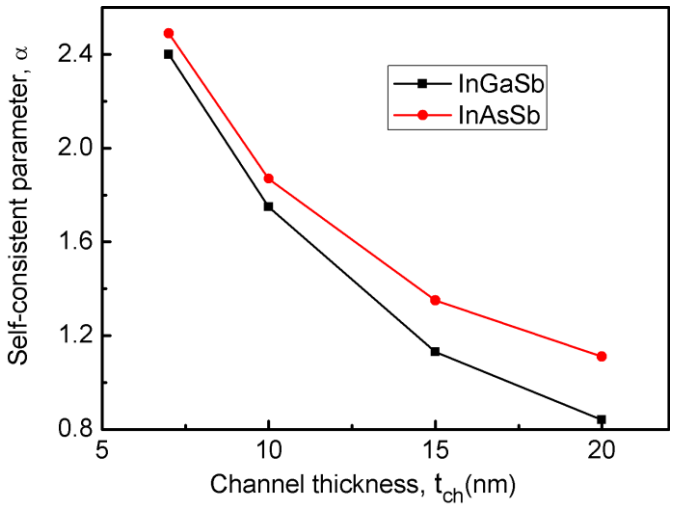


Fig. 3.3: Variation of the self-consistent parameter,α as a function of channel thickness.

When the back gate potential, V_{BG} is set to 0V, then putting $\psi_{ch} = \psi_{sf}$ and differentiating "(3.19)" with respect to V_G we get,

$$\frac{d\psi_{ch}}{dV_G} = \frac{1}{1+\frac{\varepsilon_{ch}}{t_{ch}C_{Fox}}\left(1-\frac{\varepsilon_{ch}}{\varepsilon_{ch}+t_{ch}C_{Box}}\right) - \left(\frac{1}{C_{Fox}}-\frac{\alpha}{C_{ch}}\right)\frac{4\pi g\, m^* q^2}{h^2}\sum_i \frac{e^{(E_F-E_C+q\psi_{ch}-E_i)/kT}}{1+e^{(E_F-E_C+q\psi_{ch}-E_i)/kT}}} \tag{3.20}$$

Then using "(3.6)" and "(3.20)", the gate capacitance can be expressed as

$$C_G = \frac{\frac{4\pi g\, m^* q^2}{h^2}\sum_i \frac{e^{(E_F-E_C+q\psi_{ch}-E_i)/kT}}{1+e^{(E_F-E_C+q\psi_{ch}-E_i)/kT}}}{1+\frac{\varepsilon_{ch}}{t_{ch}C_{Fox}}\left(1-\frac{\varepsilon_{ch}}{\varepsilon_{ch}+t_{ch}C_{Box}}\right) - \left(\frac{1}{C_{Fox}}-\frac{\alpha}{C_{ch}}\right)\frac{4\pi g\, m^* q^2}{h^2}\sum_i \frac{e^{(E_F-E_C+q\psi_{ch}-E_i)/kT}}{1+e^{(E_F-E_C+q\psi_{ch}-E_i)/kT}}} \tag{3.21}$$

3.4 Threshold voltage model

To improve the packing density of transistor, scaling of threshold voltage is necessary. As subthreshold leakage depends on threshold voltage, the proper choice of threshold voltage determines the overall performance of the device. Here, the threshold voltage is defined as the gate voltage required to populate the eigenenergy levels of the channel material. When $\psi_{sf} = \psi_{ch} = E_i/q$, then V_G=V_{Ti} where i is the number of eigen level. Equation "(3.19)" can be written as

$$V_{Ti} = \phi_{msf} + E_i/q + \frac{\varepsilon_{ch}E_i}{C_{Fox}t_{ch}q} - \frac{\varepsilon_{ch}}{C_{Fox}t_{ch}}\left(\frac{\frac{\varepsilon_{ch}E_i}{C_{Box}\,t_{ch}q}+\frac{qN_D}{2C_{Box}}t_{ch}-\phi_{msb}}{1+\frac{\varepsilon_{ch}}{C_{Box}\,t_{ch}}}\right) - \frac{Q_{Fch}^{QM}}{C_{Fox}} - \frac{qN_D}{2C_{Fox}}t_{ch} + \psi_{SCF} \tag{3.22}$$

when $\psi_{ch} = E_1/q$,V_G=$V_{T1}$and $\psi_{ch} = E_2/q$, V_G=$V_{T2}$and so on. Thus, using "(3.22)", multiple threshold voltages can be obtained for such UTB devices.

Chapter 4

Results and Discussions

Chapter Outlines

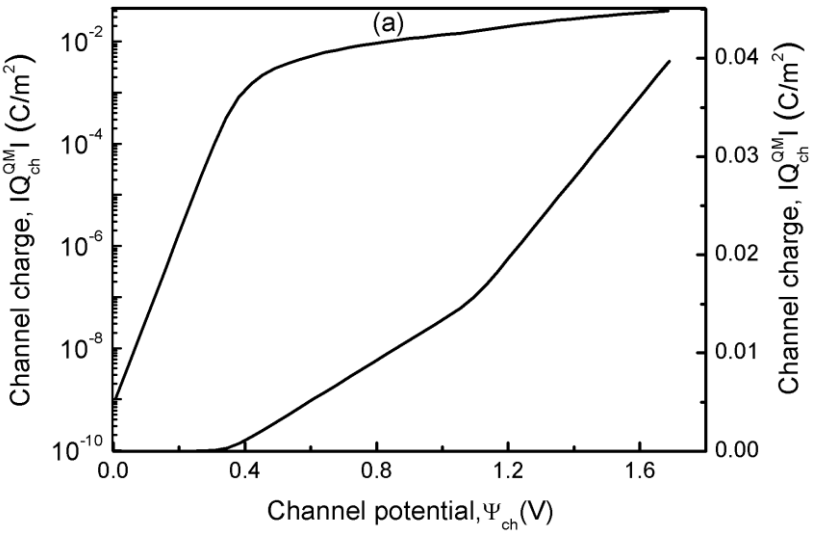
- Introduction
- Charge-voltage characteristics
- Capacitance-Voltage characteristics
    - Effect of channel thickness
    - Effect of channel doping
    - Effect of channel composition
    - Effect of temperature
    - Effect of BOX thickness
- Threshold voltage

4.1 Introduction

The charge voltage and capacitance voltage characteristics curves of ultra thin body XOI FET are very important to analyze the device performance of FET devices. The energy quantization phenomenon of UTB structure makes the C-V curves of such devices different from those of conventional FET devices. The effect of different device parameters such as channel thickness, channel composition, doping etc. on C-V curve is studied here. The multi-threshold voltage condition of such III-V materials based devices is also discussed in this section.

4.2 Charge-Voltage characteristics of XOI FET

The amount of charge at the channel determines the capacitance of MOS devices. The variation of channel charge with channel potential is shown in Fig. 4.1(a). At increased channel potential, higher eigen states start to populate which in turn increases the charge in the channel as well as the slope of the curve. The change in channel potential with gate voltage is also shown in Fig. 4.1(b). The variation of the channel potential as well as channel charge as a function of gate voltage follows multiple slope due to the gate voltage dependent population of eigen states in the channel.



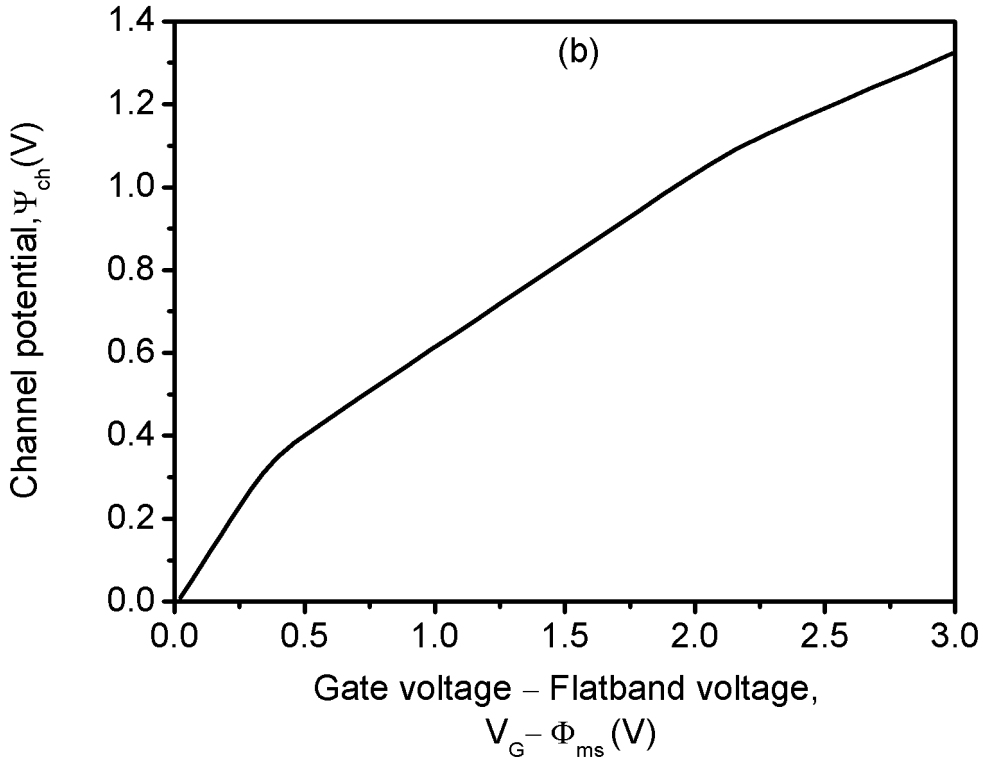


Fig. 4.1: Variation of (a) channel charge with channel potential and (b) channel potential with gate voltages of 7nm $In_{0.3}Ga_{0.7}Sb$-on-Insulator FET

4.3 Capacitance-Voltage (C-V) characteristics of XOI FET

4.3.1 Effect of channel thickness:

Unlike bulk and SOI MOSFET, XOI FET exhibits staircase nature in C-V characteristic with channel thickness as seen in Fig. 4.2(a), which arises due to the population of multiple energy subbnds with applied gate voltages. When a positive gate voltage is applied, the energy subbands go below the Fermi level and get populated. The first subband is said to be populated when the Fermi level lies in between first and second subbands. With further increase in gate voltage, the second subband goes below the Fermi level and gets populated.

As shown in Fig. 4.2(a), for 7nm channel of $In_{0.3}Ga_{0.7}Sb$-on-Insulator FET, the gate capacitance increases from 0 to 8.28fF/μm for the variation of gate voltage from $V_G = 0V$ to $V_G = 0.50\,V$ and then remain constant up to the gate voltage $V_G = 1.95V$, that is termed as

"first stair" or "first step constant-capacitance-region (CCR)" [85]. After that, with increasing gate voltage the capacitance increases from 9.54 fF/μm to 11.11 fF/μm up to the gate voltage $V_G = 2.22V$ and then remains constant up to $V_G = 3V$. This region is defined as second-step CCR. This nature of C-V is not consistent with the C-V obtained from the conventional MOSFET. The results obtained from the analytical model are compared with the numerical analysis (SILVACO ATLAS) which shows an excellent agreement for 7nm and 10 nm channel thickness. But for 15nm and 20nm channel thickness a reasonable agreement is found. It is attributed to the fact that at this thickness the staircase nature almost disappears and acts like conventional SOI MOSFET. The reason for staircase disappearance is that the energy difference between the eigen states reduces at increased channel thickness, which leads to have easy movement of carriers in energy subbands [85]. Both the numerical and analytical results suggest that the staircase nature completely disappears at a channel thickness of 20nm.

To confirm the generalized characteristics of the model it is further applied to study the C-V characteristics of $InAs_{0.7}Sb_{0.3}$-on-Insulator FET. Fig. 4.2(b) shows that the analytical and numerical results are in excellent agreement and show the same trend as $In_{0.3}Ga_{0.7}Sb$-on-Insulator FET. However, in the later case a higher gate voltage is required to populate the channel owing to the low effective mass of $InAs_{0.7}Sb_{0.3}$-on-Insulator FET. The staircase nature in this case also almost disappears at a channel thickness of 20nm.

Fig. 4.2(a) and (b) also show that, for the positive gate voltage, the C-V curve shifts toward left with increasing channel thicknesses. As the energy eigen value of each subband reduces with increasing channel thickness, the difference between 1^{st}eigen and E_F at zero gate bias reduces. As a result, lower gate voltage is required to populate the 1^{st}eigen level, resulting the left shift in 1^{st} step CCR. Similarly, reduction of energy of the 2^{nd}eigen and Fermi level causes the left shift in 2^{nd} step CCR. The reduction of the difference between 1^{st} and 2^{nd}eigen

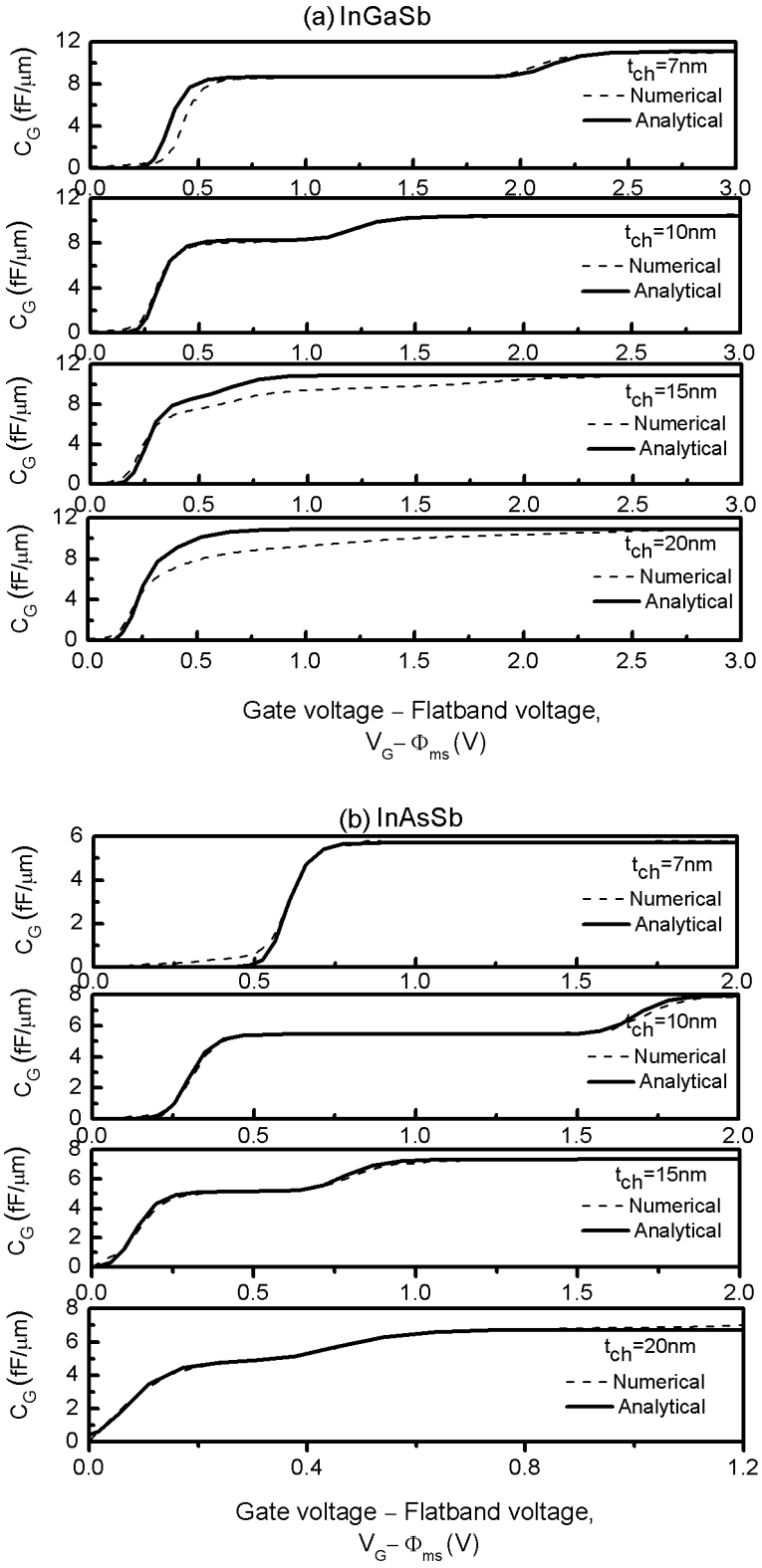


Fig. 4.2: Comparison between analytical (solid lines) and numerical (dotted lines) results (a)$In_{0.3}Ga_{0.7}Sb$-on-Insulator FET and (b) $InAs_{0.7}Sb_{0.3}$-on-Insulator FET at different channel thicknesses.

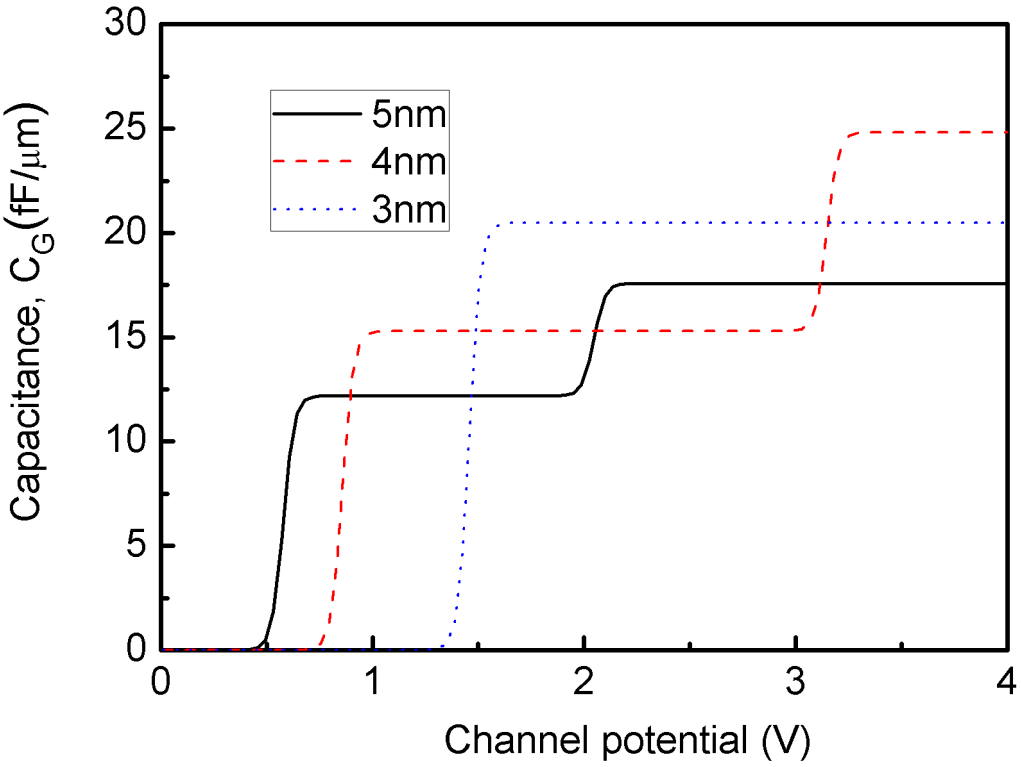


Fig. 4.3: Channel potential dependent capacitance of $In_{0.3}Ga_{0.7}Sb$-on-Insulator FET at channel thicknesses of 3nm, 4nm and 5nm .

energies causes the width of the 1st step CCR to be smaller at higher channel thickness.

Fig. 4.3 shows the variation of channel capacitance of $In_{0.3}Ga_{0.7}Sb$-on-Insulator FET at channel thicknesses of 3nm to 5nm. It is also seen that at reduced channel thickness higher gate voltage is required to invert the channel. Although the device carries the essential physics of such devices, the value of self-consistent parameter needs to be adjusted for exact capacitance value.

4.3.2 Effect of Channel Doping:

Fig. 4.4(a) and (b) show the doping concentration dependent shifts in C-V curve of $In_{0.3}Ga_{0.7}Sb$-on-Insulator FET and $InAs_{0.7}Sb_{0.3}$-on-Insulator FET. As the doping density increases, the difference between energy eigen level and the Fermi energy decreases. This causes a left shift in the C-V curves. The value of the eigen energy does not depend on the channel doping, so it neither affects the staircase nature nor the width of 1st or 2nd step CCR of

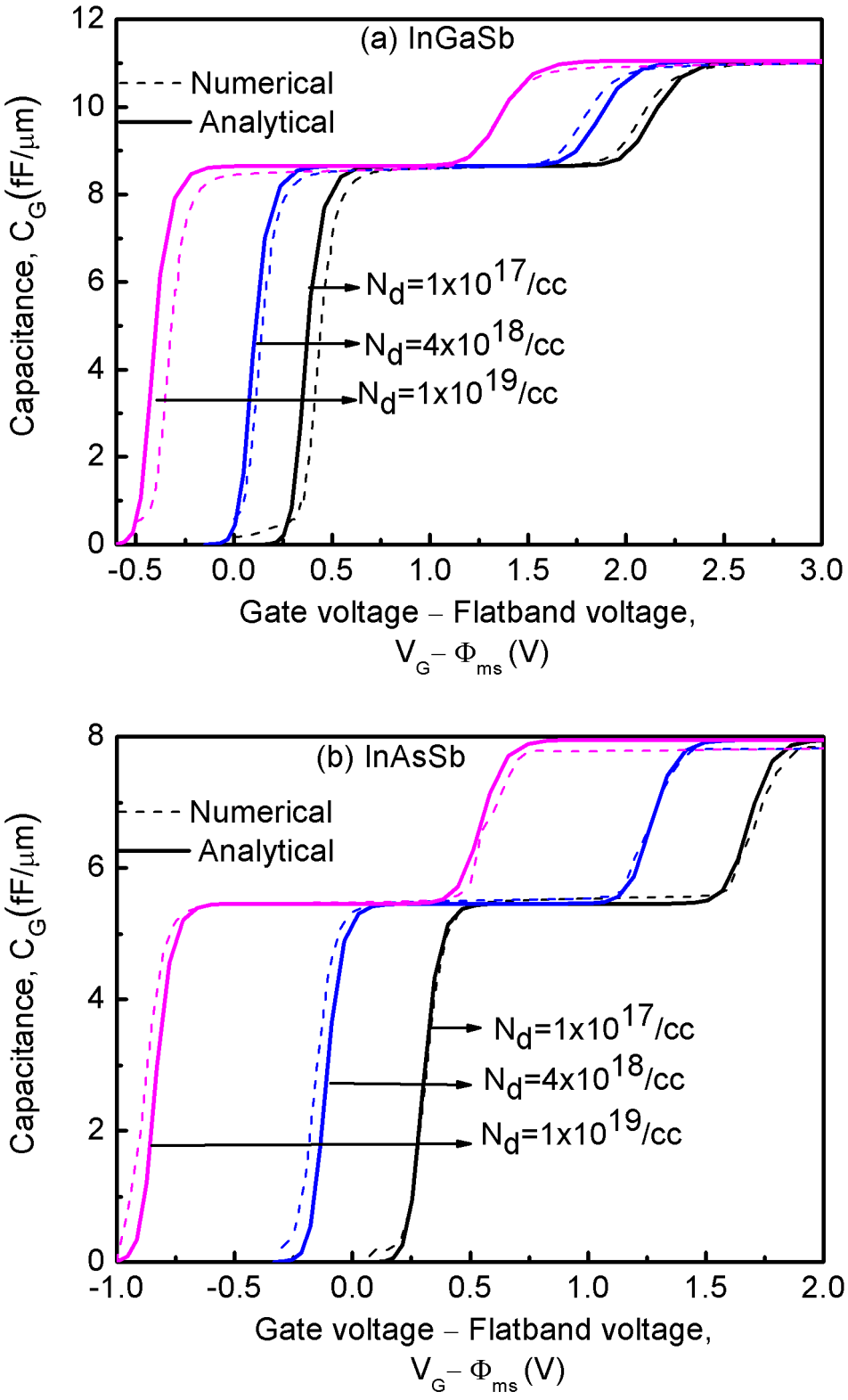


Fig. 4.4: Comparison between analytical (solid lines) and numerical (dotted lines) results (a) $In_{0.3}Ga_{0.7}Sb$-on-Insulator FET and (b) $InAs_{0.7}Sb_{0.3}$-on-Insulator FET at different doping concentration.

the C-V characteristics. The numerical and analytical results show good agreement in both cases. Note that our analytical model is general. Beside InGaSb and InAsSb XOI, the model

can be used to study the C-V characteristics of ultra thin body XOI FET with other III-V materials in the channel as well.

4.3.3 Effect of Channel Composition:

Fig. 4.5 shows the composition dependent C-V curve of XOI FET. The capacitance is found to have composition dependence and changes rapidly with gate voltage upto V_G=0.5V. Then, with increasing gate voltage the capacitance in both 1st and 2nd step CCR increases for increased Ga composition. This is owing to the fact that the density of state increases with increased Ga composition. Also, the differences between 1st and 2nd eigen state decreases with increasing Ga composition. As a result lower gate voltage is required for transition from 1st to 2nd step CCR which causes a left shift of the C-V curve.

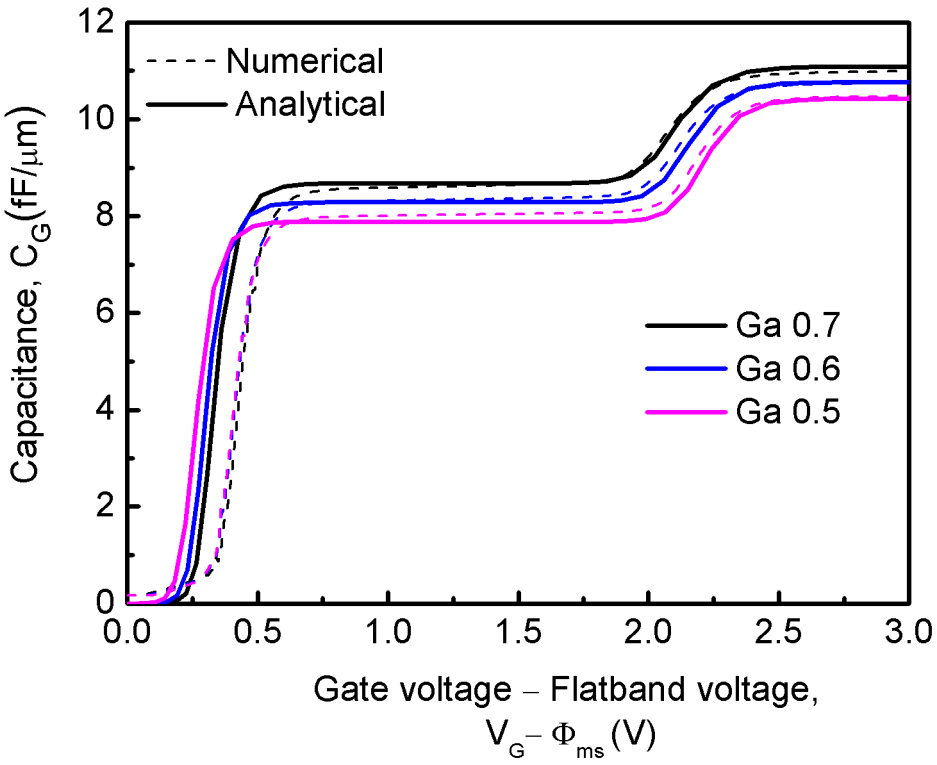


Fig. 4.5: Comparison between analytical (solid lines) and numerical (dotted lines) results of $In_{0.3}Ga_{0.7}Sb$-on-Insulator FET at different channel material composition.

4.3.4 Effect of Temperature:

Effect of temperature on C-V curve is shown in Fig. 4.6. It is seen that temperature has no effect on 1st and 2nd step CCR because the eigen energy is independent of temperature. Also, the thermal voltage (.026V) is very low in comparison to the energy difference between Fermi level and 1steigen level as well as the difference between 1st and 2ndeigen level. The slope of the transition from minimum point to 1st step CCR and so from 1st step to 2nd step CCR becomes steeper at reduced temperature which leads to better subthreshold slope hence better turn on characteristics.

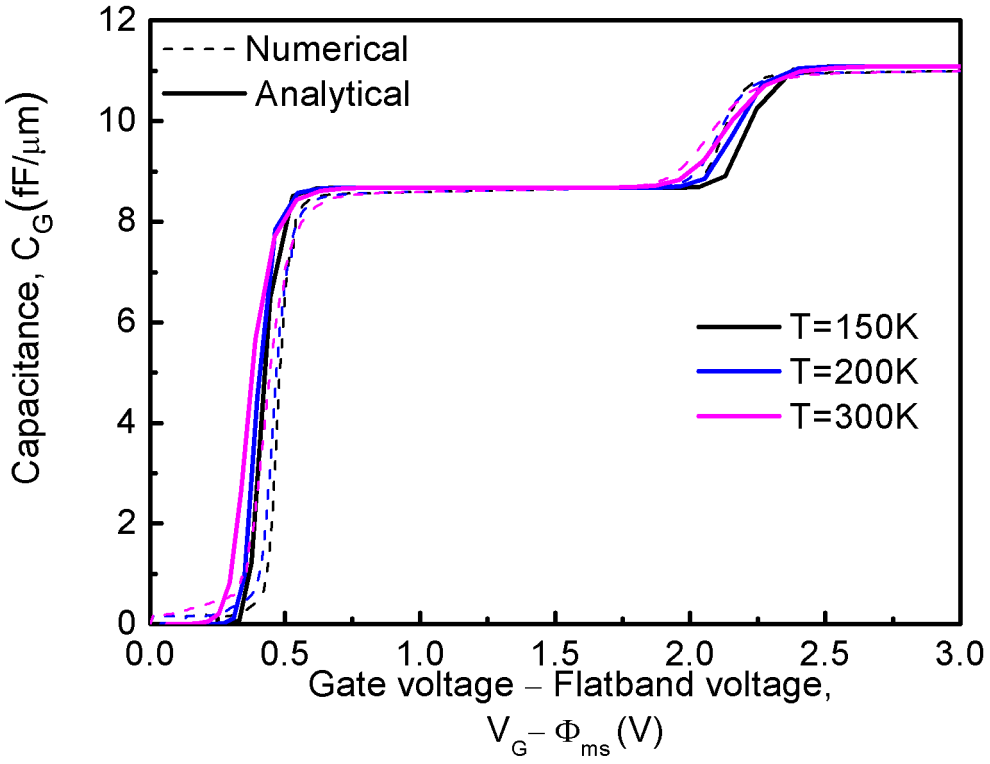


Fig. 4.6: Comparison between analytical (solid lines) and numerical (dotted lines) results of $In_{0.3}Ga_{0.7}Sb$-on-Insulator FET at different temperature.

4.3.5 Effect of BOX thickness

Figure 4.7 shows the effect of box thickness on C-V curve of $In_{0.3}Ga_{0.7}Sb$-on-Insulator FET for 7nm to 20nm box thicknesses. Change of BOX thickness doesn't change the eigen levels. Hence the overall capacitance remains almost constant. Although, a small variation in the second eigen level is observed in the analytical graph due to a higher variation of the channel potential with gate voltage, $\frac{d\psi_{ch}}{dV_G}$. The values of the self-consistent parameter at different box thickness are shown in Fig. 4.6(c).

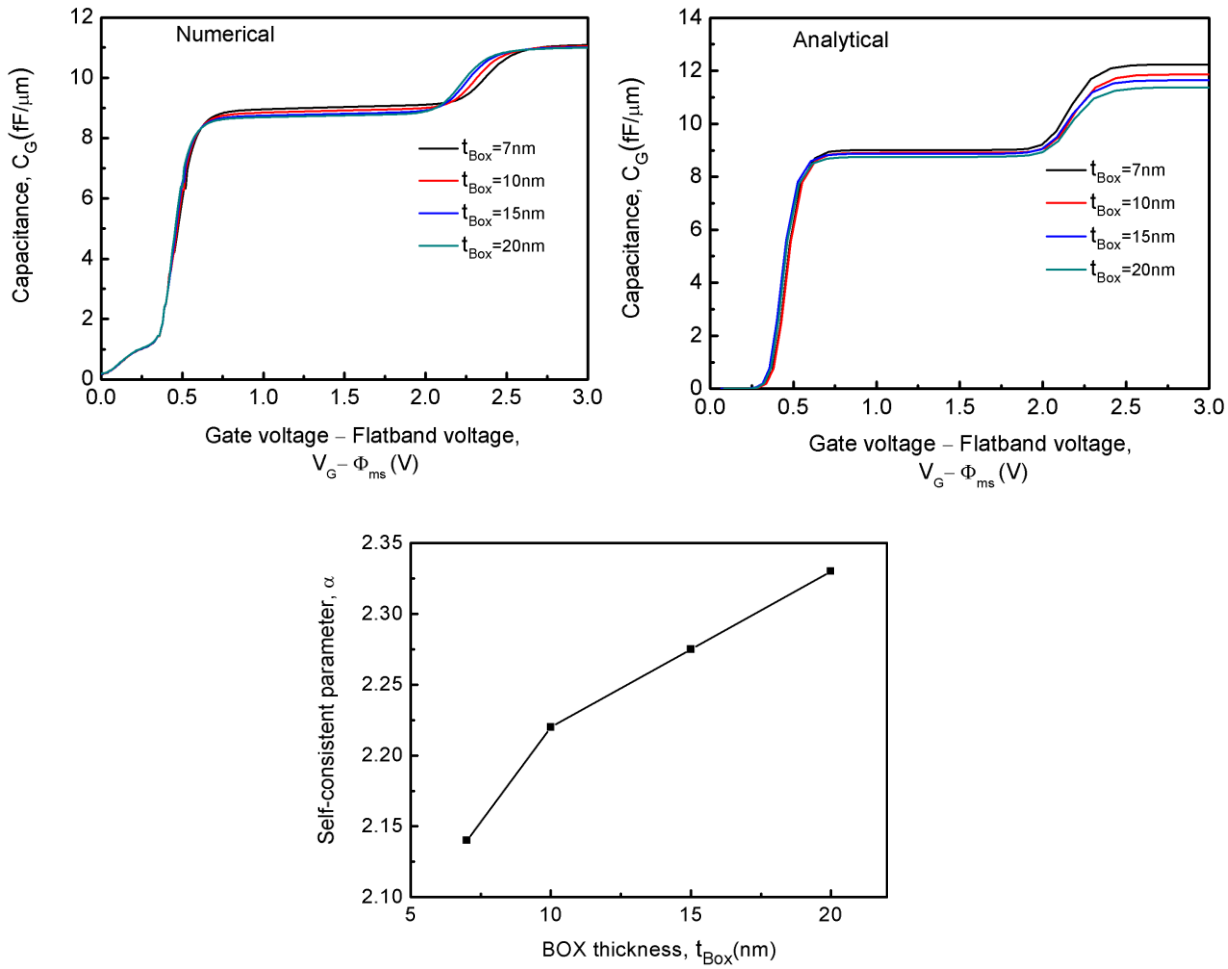


Fig. 4.7: Comparison between (a) numerical and (b) analytical results of $In_{0.3}Ga_{0.7}Sb$-on-Insulator FET at different box thicknesses and (c) variation of self-consistent parameter at different box thicknesses.

4.4 Threshold Voltage

In CMOS, multi-threshold condition is important for the optimization of device power and switching delay. Using multi-threshold condition low power MOS devices has been proposed [86] and also using this concept MOS current mode Ex-OR gate [87] has been implemented. Also, the concept of high speed voltage flip flops using multi threshold condition [88] has been studied. Here, the gate voltage at which 1st and 2nd eigen state populates is termed as V_{T1} and V_{T2}, respectively. The variation of threshold voltage with channel thickness is calculated using (3.22) and shown in Fig. 4.8. At lower channel thickness, the value of the eigen energy level is higher. Hence, higher gate voltage is required to invert the channel. So, the threshold voltage is higher at reduced channel thickness.

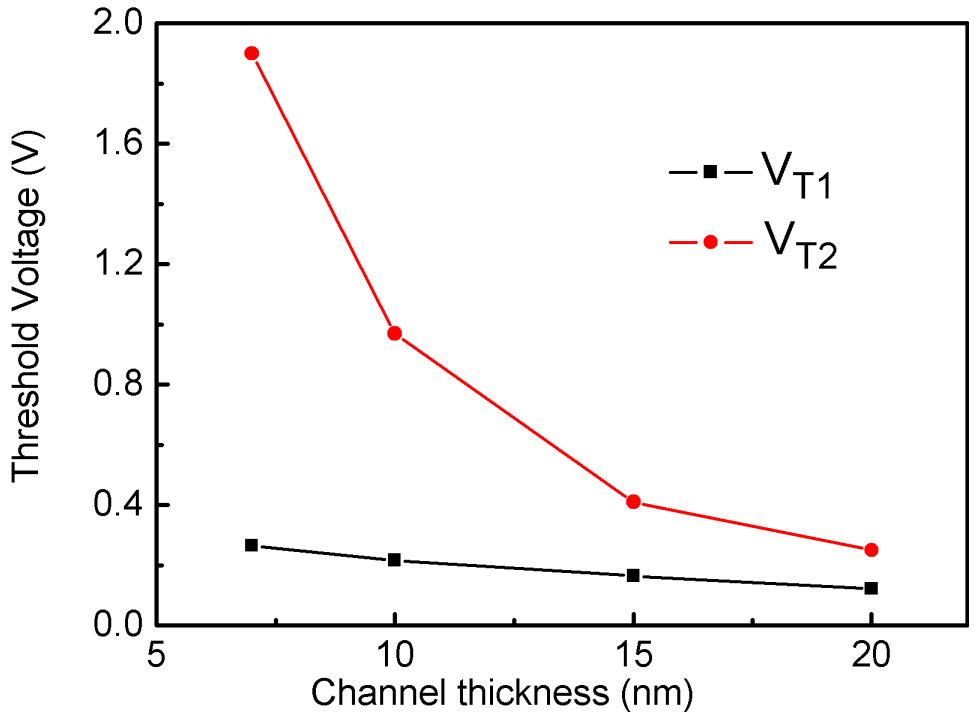


Fig. 4.8: Threshold voltage of $In_{0.3}Ga_{0.7}Sb$-on-Insulator FET at different channel thicknesses.

Chapter 5

Concluding Remarks

Chapter Outlines

- Conclusion
- Recommendation for future work

5.1 Conclusion

A generalized analytical model is developed here that can suitably explain the gate voltage dependent C-V characteristics of III-V based ultra thin body XOI FET. To investigate the accuracy of the model, we have compared analytical results with numerical calculations from Silvaco Atlas.It is found that the C-V characteristics of ultra thin body XOI FET possess a unique staircase nature due to quantum confinement effect. The gate capacitance varies from 0 to 8.28fF/µm for gate voltage variation of $V_G = 0V$ to $V_G = 0.50\,V$ and then remain constant up to the gate voltage$V_G = 1.95V$ that is termed as first step CCR. After that, with increasing gate voltage the capacitance increases from 9.54 fF/µm to 11.11fF/µm up to the gate voltage $V_G = 2.22V$and then remains constant up to $V_G = 3V$. The second constant step region is termed as second step CCR. This nature almost disappears when channel thickness become more than 20nm and resembles like traditional MOS devices. It is seen that the doping concentration does not effect the capacitance because the eigen energy does not depend on channel doping. But, the reduction of energy differences between eigen energy level and Fermi level with gate voltage causes a left shift of C-V curve.For increased Ga composition of InGaSb based XOI FET, the value of capacitance is found higher due to the increased density of states. The reduced energy differences between $1^{st}$and 2^{nd} eigen level at increased Ga composition causes a left shift in C-V curve. Temperature and box thickness has very little impact on C-V curve because the eigen energy is independent of both temperature and box thickness. It is also seen that, the staircase nature of C-V curve allows to extract muli-threshold voltage which is important for improved device performance. At reduced channel thickness, the eigen energy level is higher. So, higher gate voltage is required to invert the channel which leads to higher threshold voltage at reduced channel thickness.

5.2 Recommendation for future work

The future research can be extended by including theeffect of interface trap sates, fixed oxide charge on C-V curve of XOI FET.The effect of drain/source and substrate capacitance on C-V curve can also be studied.An analytical model for the current-voltage characteristics curve of such devicescan be developed.Prospect of other emerging materialsuch as molybdenum disulfide (MoS_2) on device characterictics can also be studied.

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